NANOELECTRONICS AS INNOVATION DRIVER FOR A GREEN SUSTAINABLE WORLD

Cor Claeys

imec


HUMAN++++
TECHNOLOGY
IN EVERY ASPECT OF OUR LIFE


4.5 BILLION CELL PHONES


SMART PHONE
EASY TO USE INNOVATIVE APPS


54 MILLION UNITS IN 2011
208 MILLION BY 2014
2011 EXPLOSION TABLET PC




SAMSUNG

ASUS



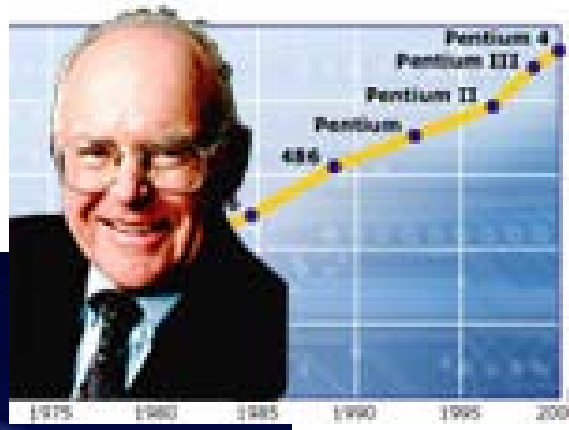

LifeTouch

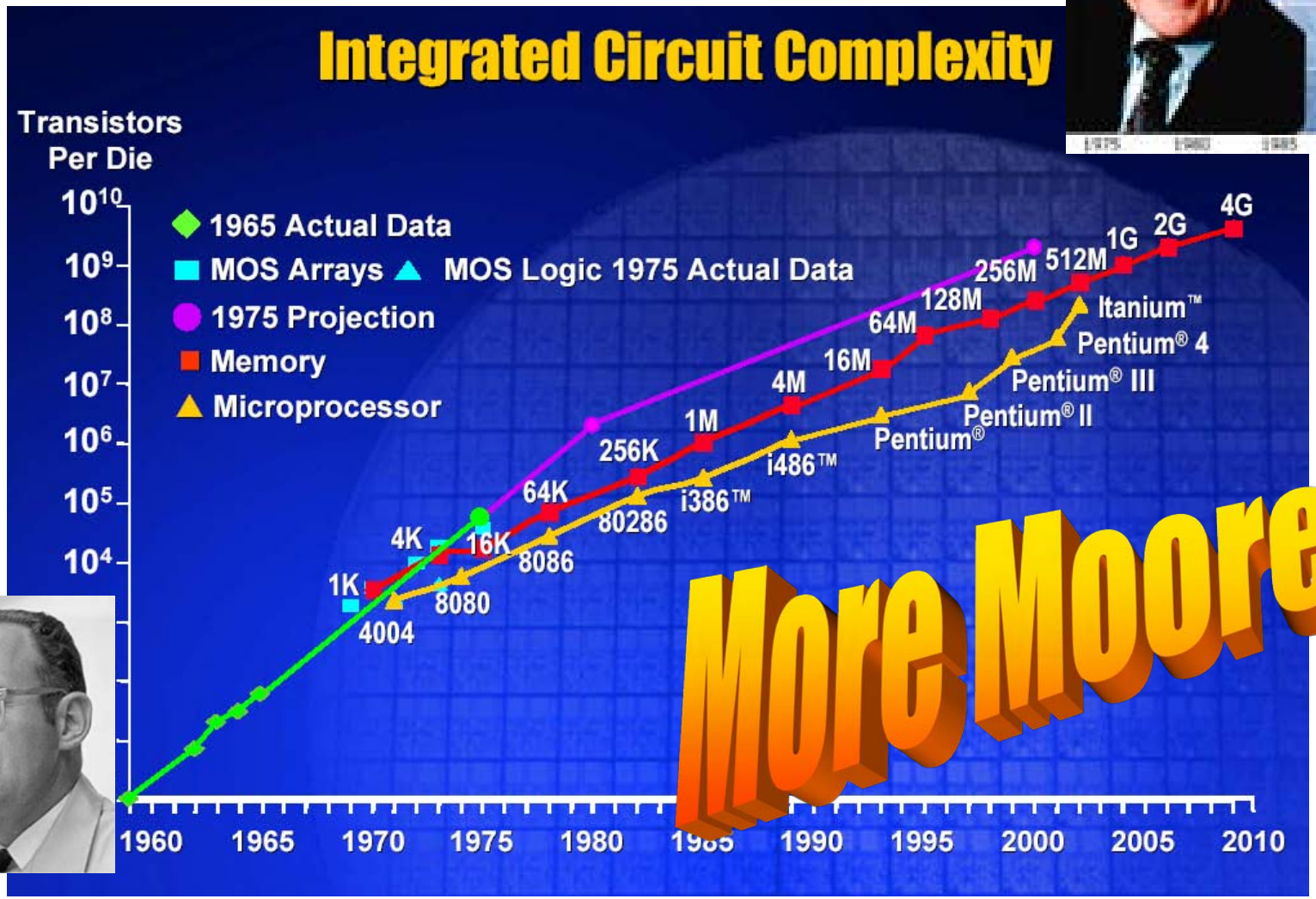

msi


qik

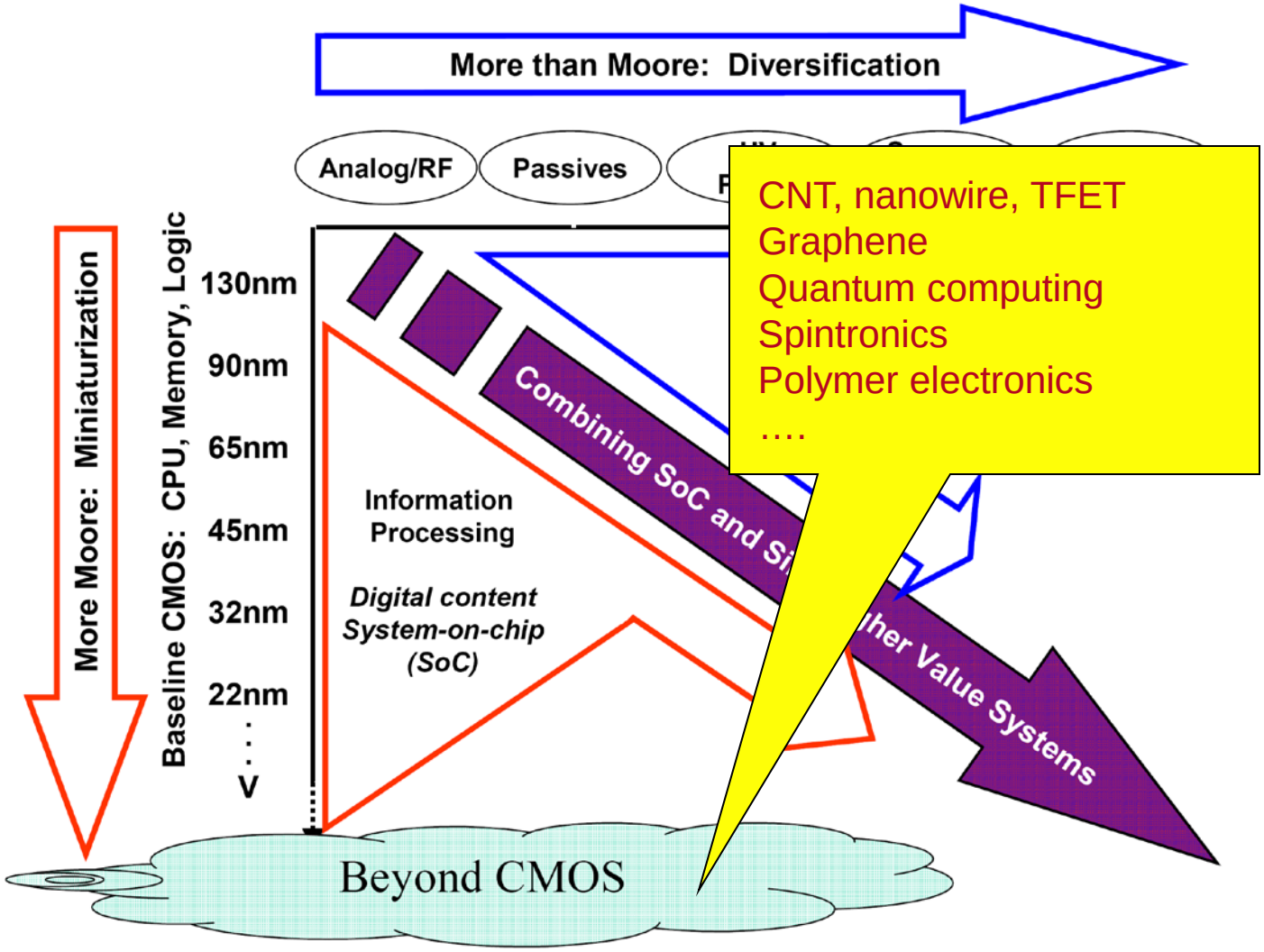
SMARTER MOBILITY
ROAD VIEW TRANSMITTING SYSTEM

KEEP INCREASE OF THE NUMBER OF COMPONENTS.
COST PER COMPONENTS DECREASES!

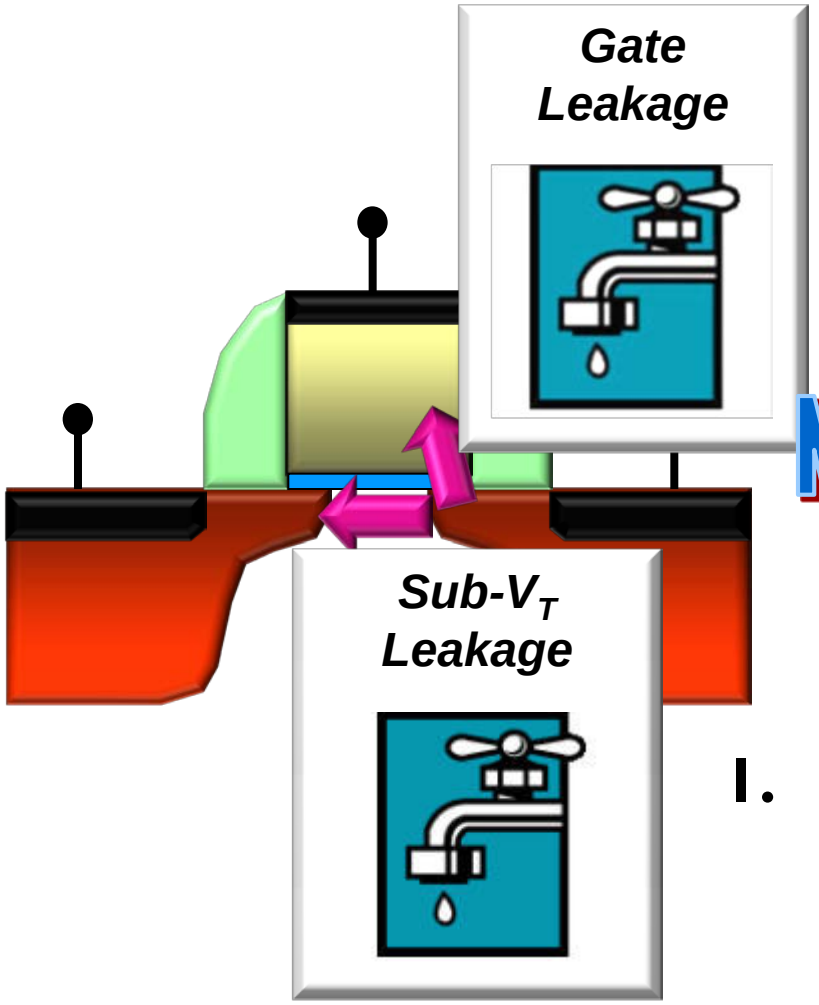




TECHNOLOGY ROADMAP: STRATEGIC AGENDA



SCALING HAMPERED BY LEAKAGE CURRENTS



2. Gate oxide leakage or Tunneling current

– As oxide thins down, leakage increases exponentially

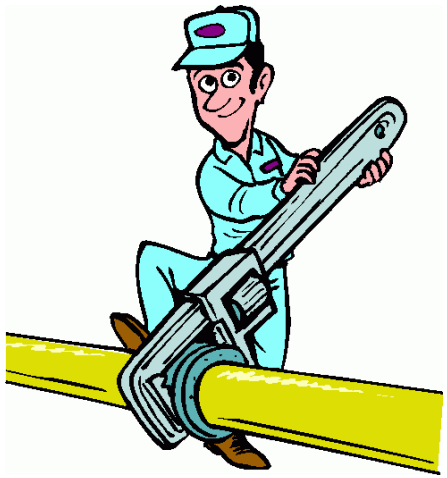
Need new materials and/or new architectures !

1. Subthreshold leakage

- Shorter channel lengths
- Threshold voltage not scaling as fast as V_{DD}

TACKLING THE POWER PROBLEM

Gate Leakage



<u>Solution</u> → New Material

e.g., **High-K** dielectric

TACKLING THE POWER PROBLEM

Gate Leakage

Solution → New Material
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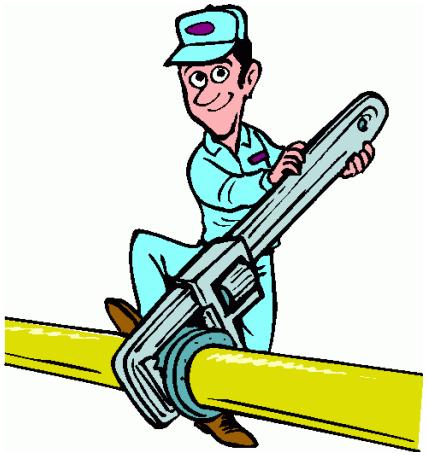


Sub-V_T Leakage

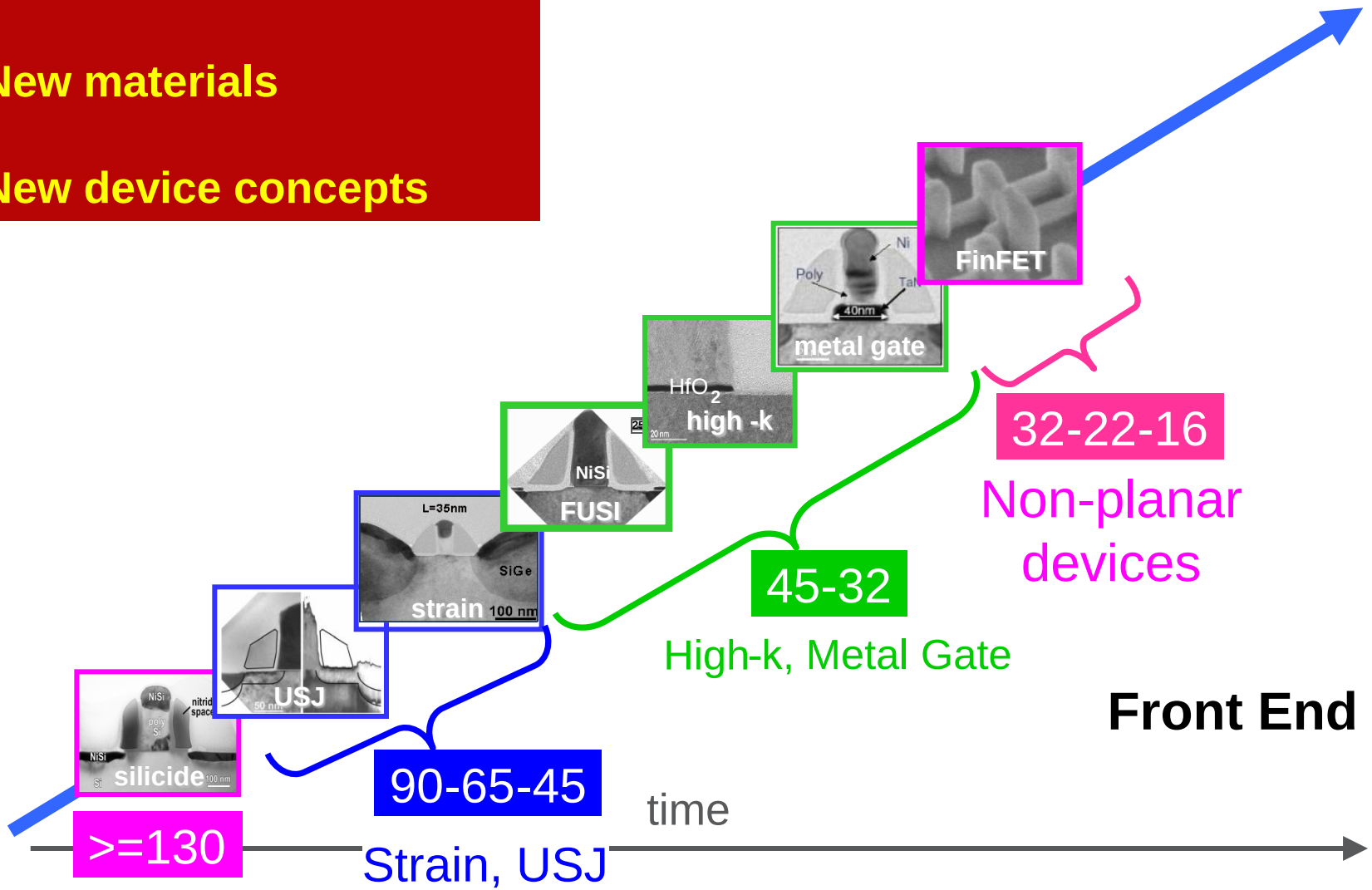
Solution → New Architecture
e.g., **Fully Depleted Devices**
for better
Short-Channel control

TRANSISTOR SCALING

New process modules

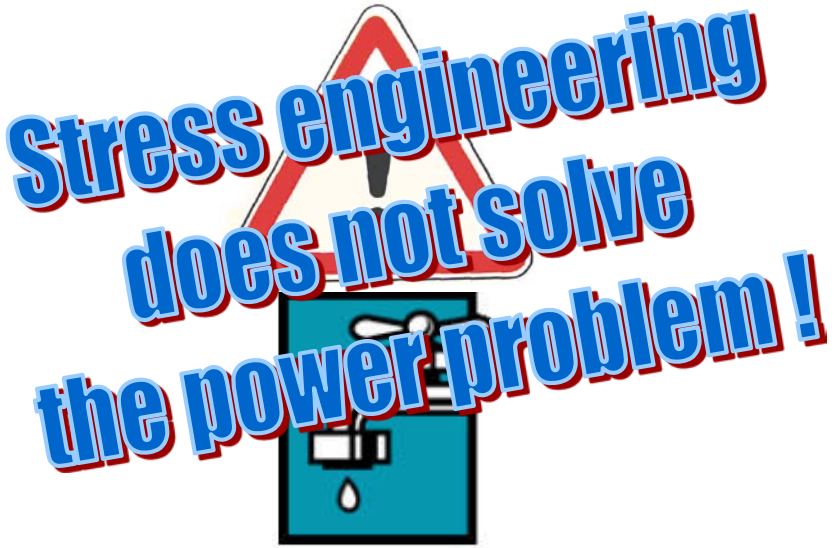
New materials

New device concepts



STRESS ENGINEERING :A DRIVING FORCE

…	90nm	65nm	45nm	32nm
		• SMT^{x1}	• SMT^{x2}	• SMT^{x3}
	• e-SiGe + tCESL • (100)/[100] + tCESL	• e-SiGe + tCESL • (100)/<100> + tCESL • DUAL CESL	• e-SiGe + tCESL • e-SiGe + DUAL CESL • DUAL CESL	• e-SiGe + tCESL • e-SiGe + DUAL CESL • DUAL CESL
			• SPT (Stress Proximity Technique)	• SPT (Stress Proximity Technique)
			• *(Surface Engineering: (110)/<110> pMOS; (100)/<100> nMOS)*	• Surface Engineering: (110)/<110> pMOS (100)/<100> nMOS
				• e-SiC

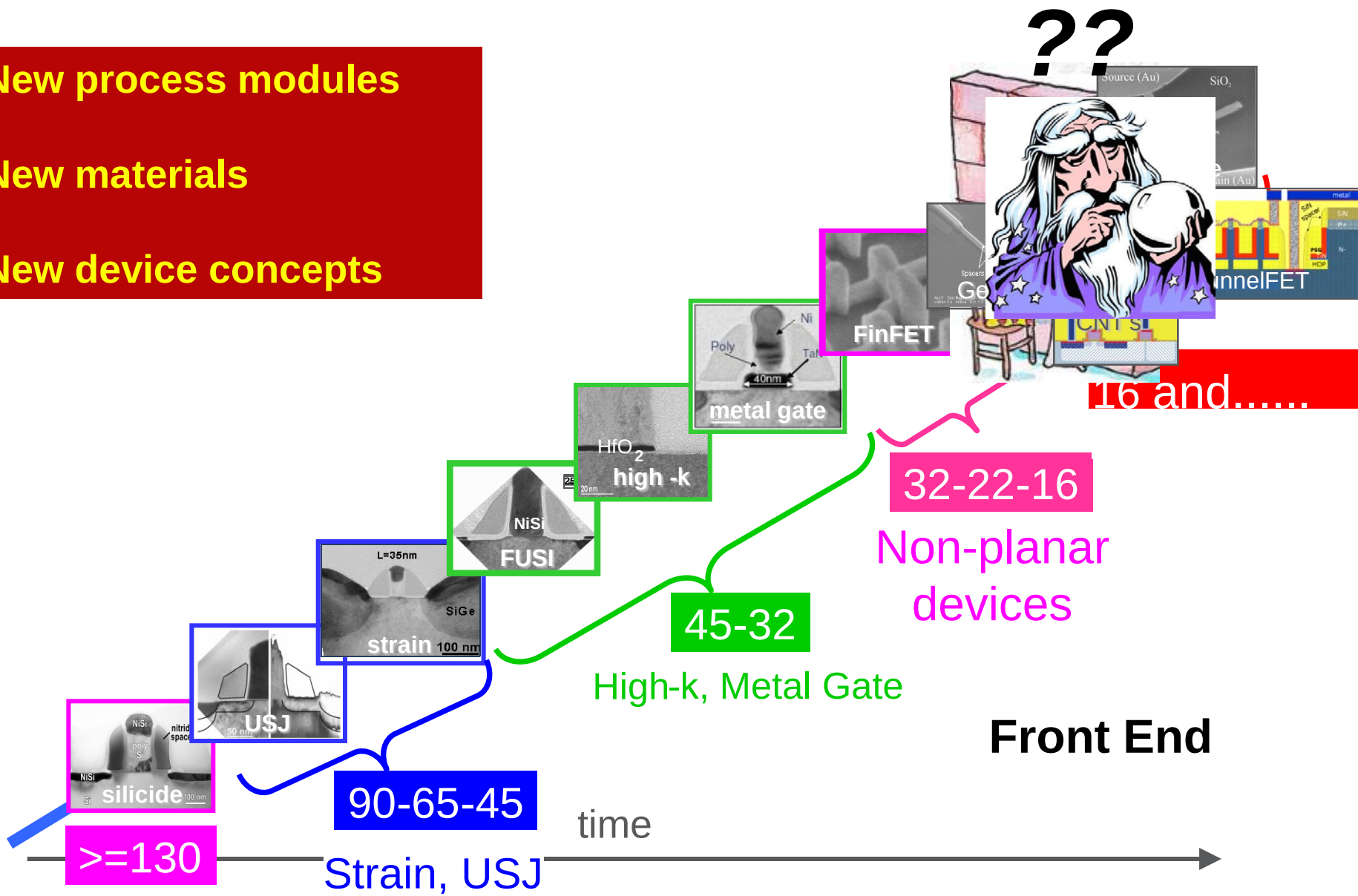


TRANSISTOR SCALING

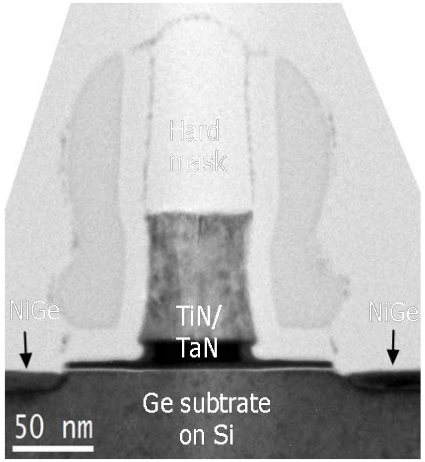
New process modules

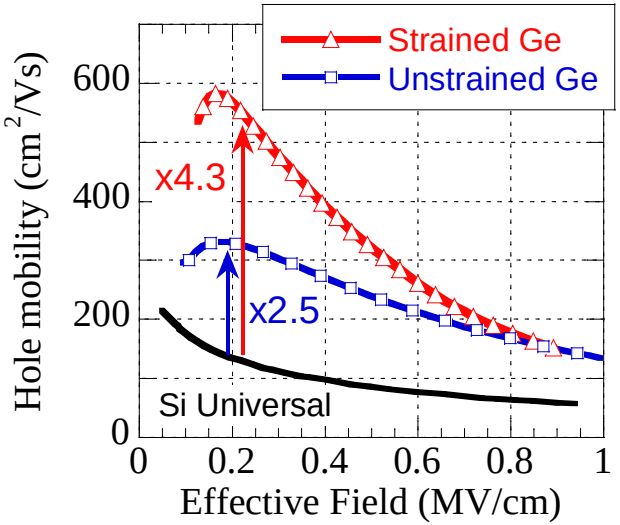
New materials

New device concepts

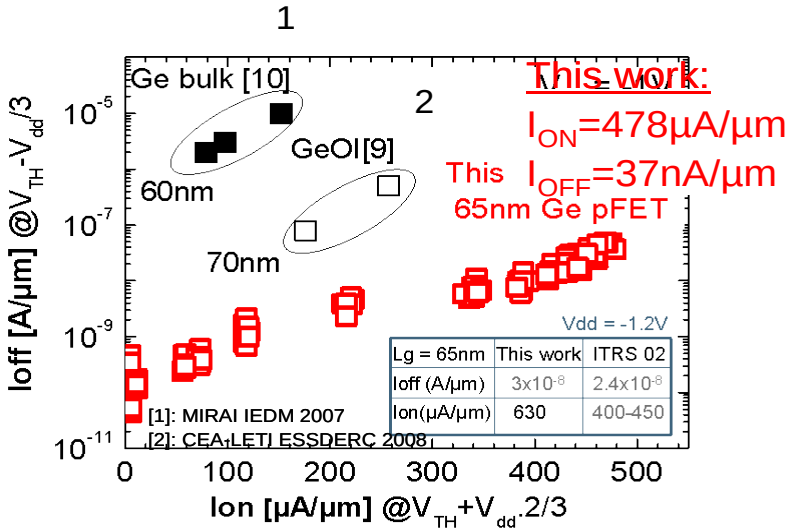


Ge PMOS

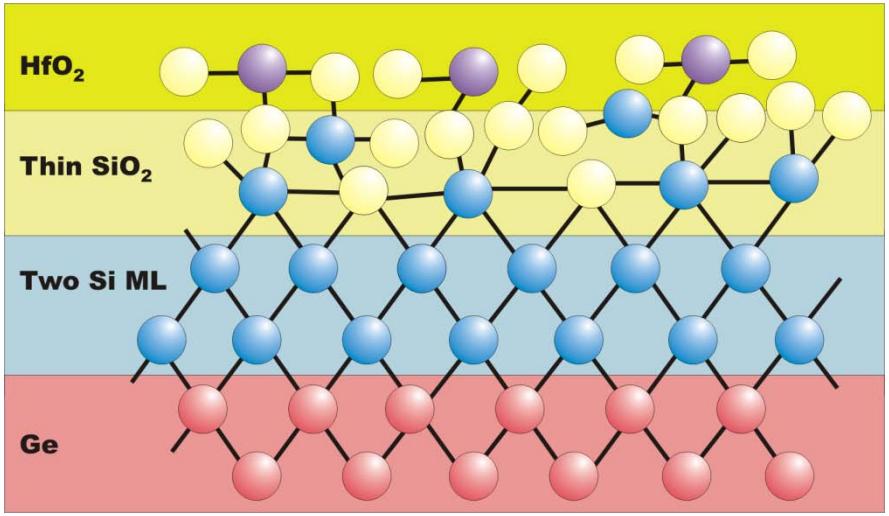


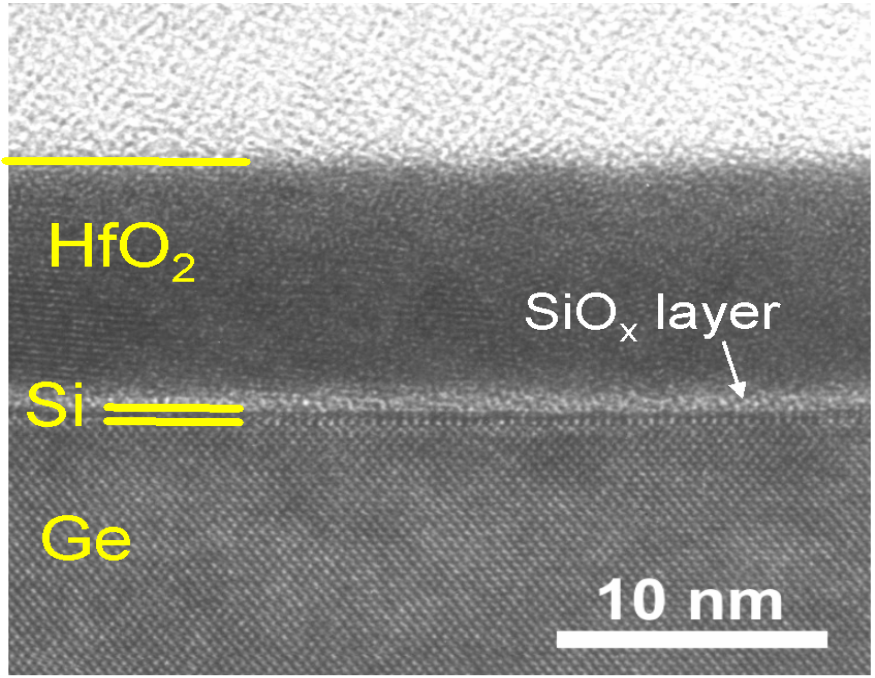


J. Mitard et al., IEDM 2008, p. 873

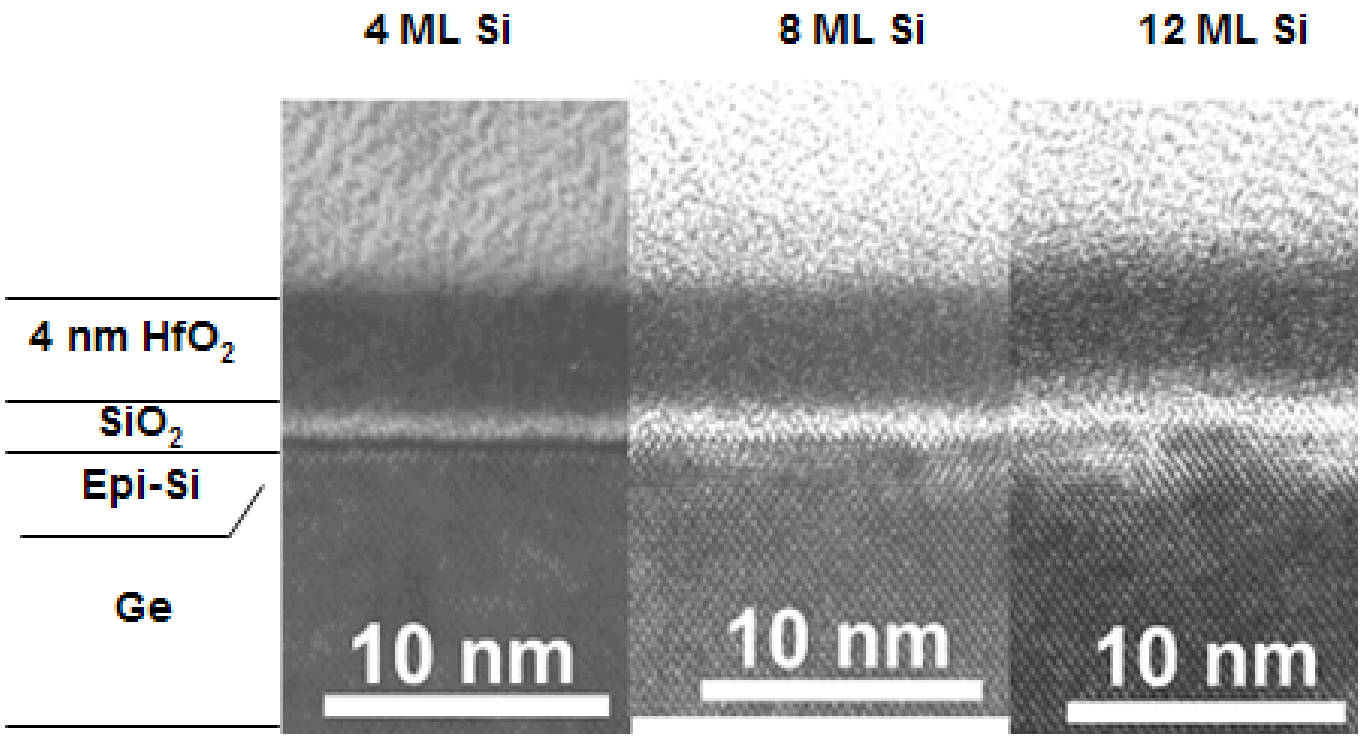


Ge PMOS – INTERFACE ENGINEERING



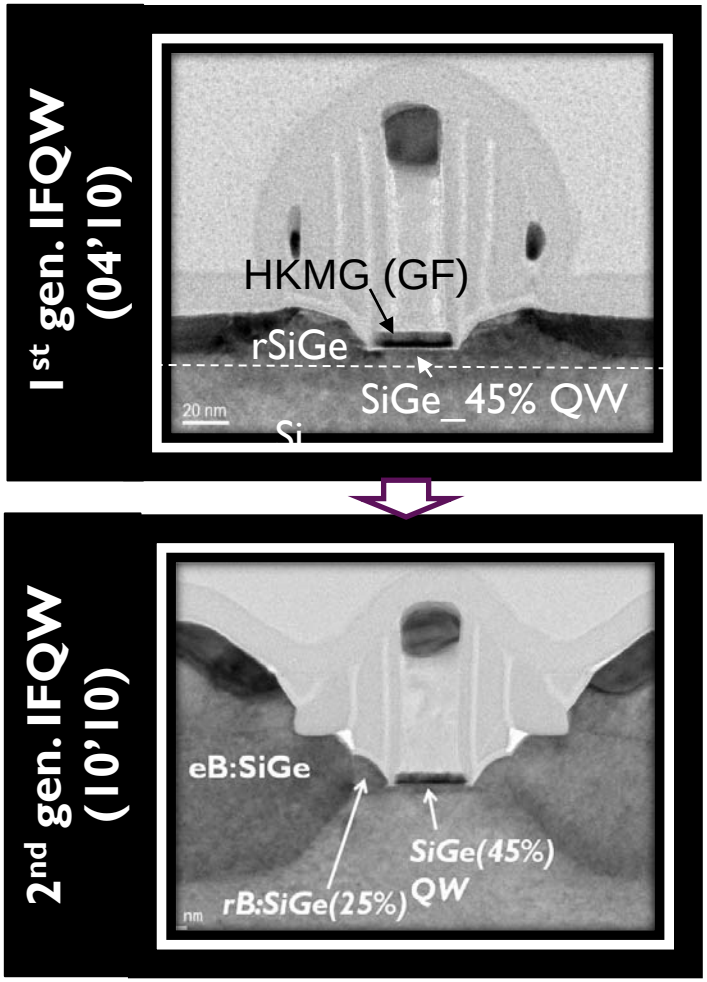


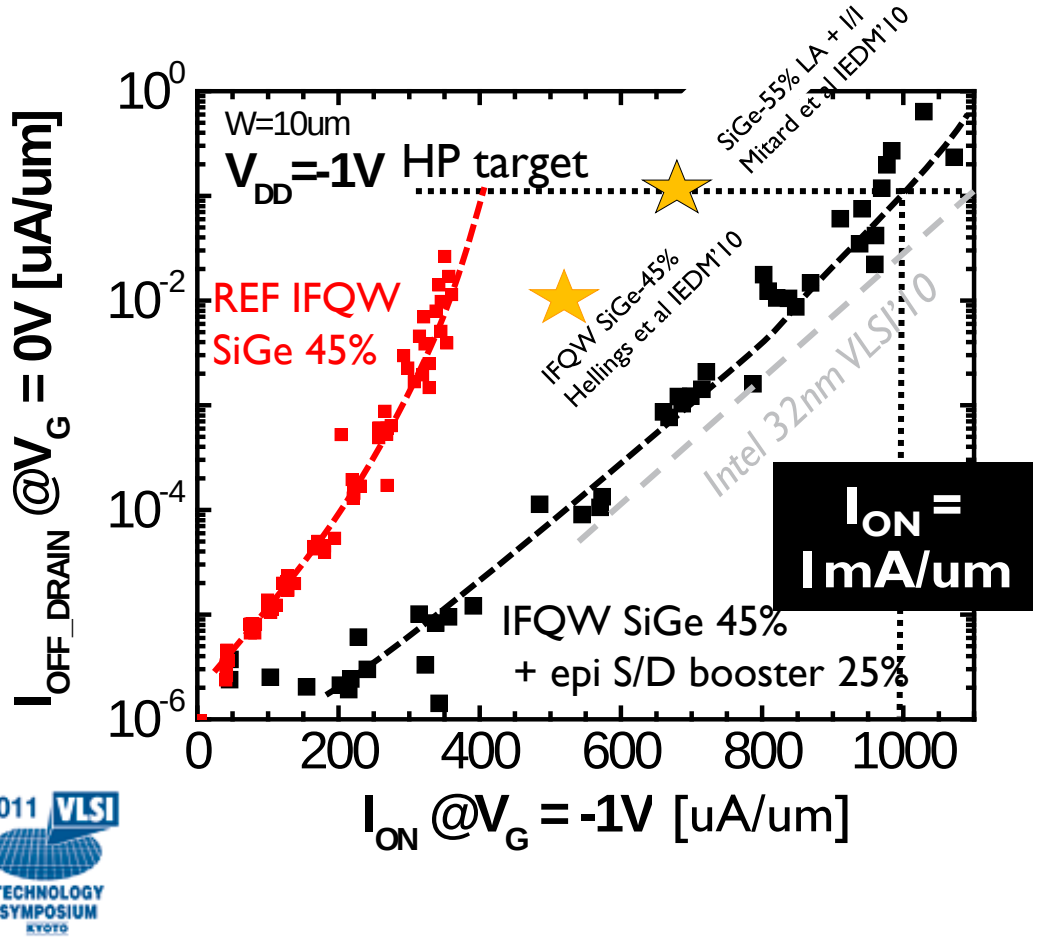
Ge DEVICES – SURFACE PASSIVATION



Cross-sectional TEM images of a high-k gate stack on a Ge surface passivated by different thicknesses of Si. At 12 MLs of silicon, the layer relaxes, giving rise to misfit dislocations at the interface.

HIGH-MOBILITY GE-BASED IMPLANT-FREE QUANTUM WELL DEVICES





2011 VLSI TECHNOLOGY SYMPOSIUM KYOTO

2nd generation SiGe QW with additional eSiGe S/D booster achieved extremely ***high performance*** (Ion=1mA/um) combined with intrinsically ***superb Short-Channel control*** (DIBL ~ 130mV/V, Lg ~ 30nm)

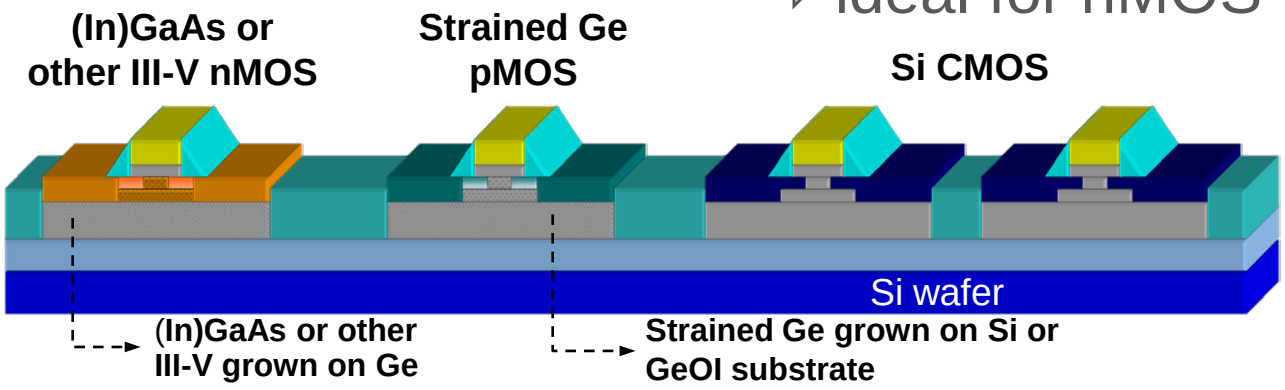
CMOS WITH HIGH-MOBILITY CHANNEL MATERIALS

S. Takagi, The University of Tokyo, INC4 2008

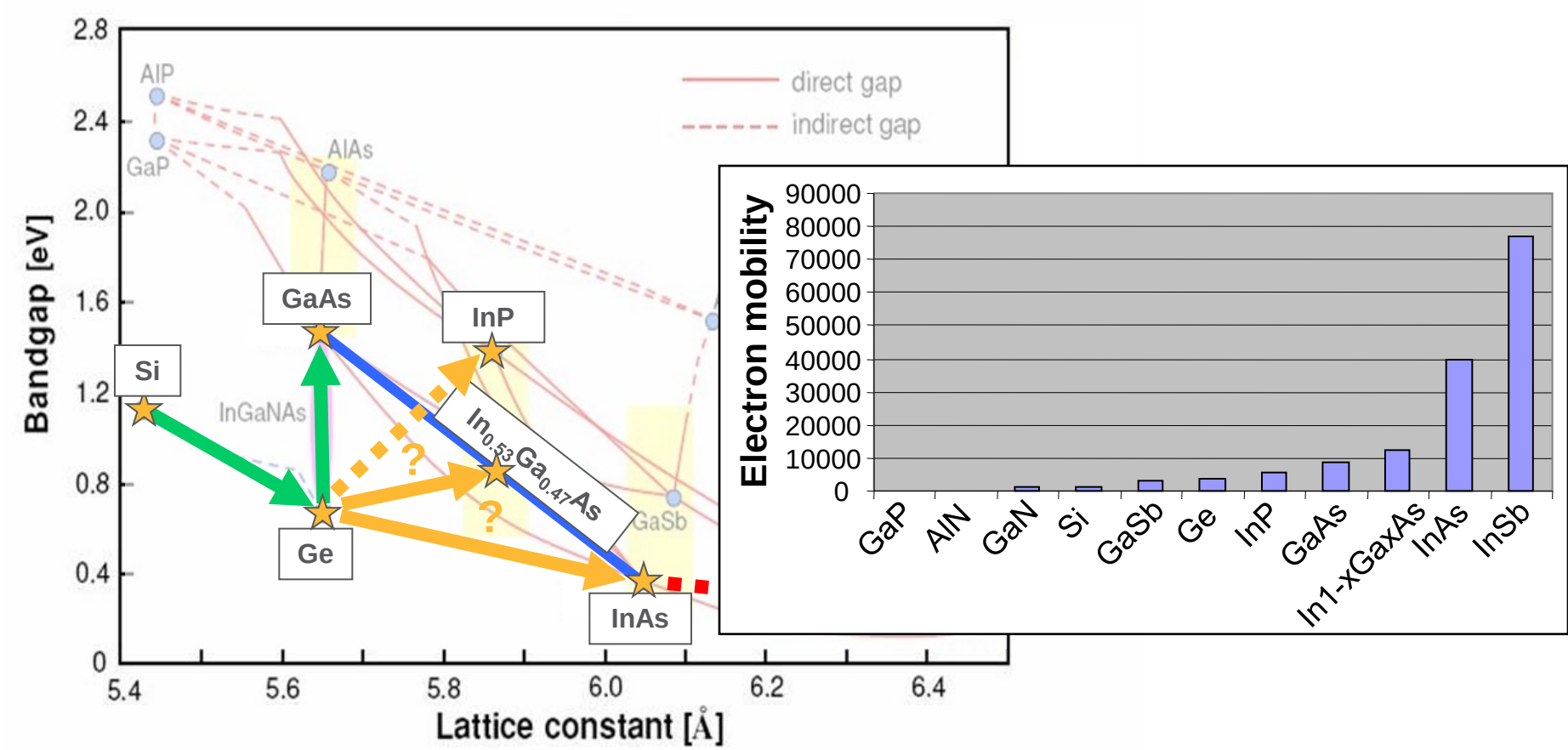
	Si	Ge	GaAs	InP	InAs	InSb
electron mob. (cm^2/Vs)	1600	3900	9200	5400	40000	77000
electron effective mass ($/m_0$)	m_t: 0.19 m_l: 0. 916	m_t: 0.082 m_t: 1.467	0.067	0.082	0.023	0.014
hole mob. (cm^2/Vs)	430	1900	400	200	500	850
hole effective mass ($/m_0$)	m_{HH}: 0.49 m_{LH}: 0.16	m_{HH}: 0.28 m_{LH}: 0.044	m_{HH}: 0.45 m_{LH}: 0.082	m_{HH}: 0.45 m_{LH}: 0.12	m_{HH}: 0.57 m_{LH}: 0.35	m_{HH}: 0.44 m_{LH}: 0.016
band gap (eV)	1.12	0.66	1.42	1.34	0.36	0.17
permittivity	11.8	16	12	12.6	14.8	17

- Ge has lightest hole m*
  ⇨ good for pMOS
- Many III-V materials have light electron m*
  ⇨ ideal for nMOS

Combination of high mobility III-V nMOS and (strained) Ge pMOS integrated on Si substrate for ultimate CMOS performance



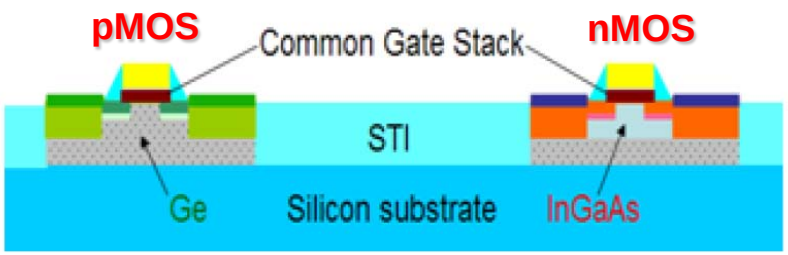
Ge AS INTERMEDIATE SEMICONDUCTOR

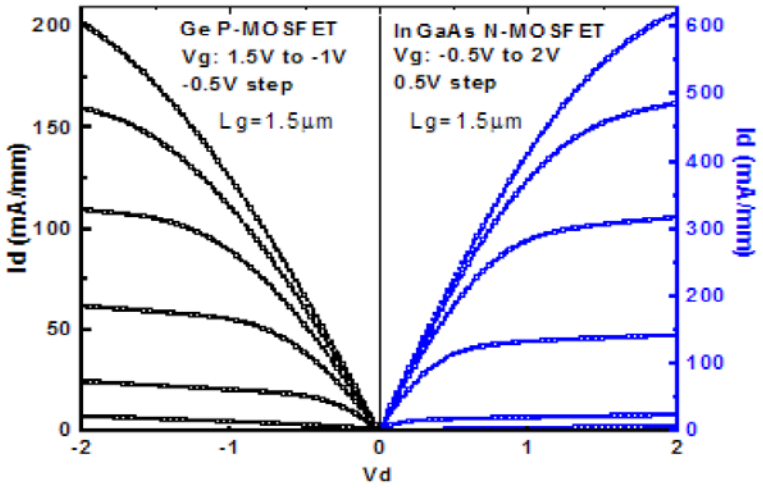


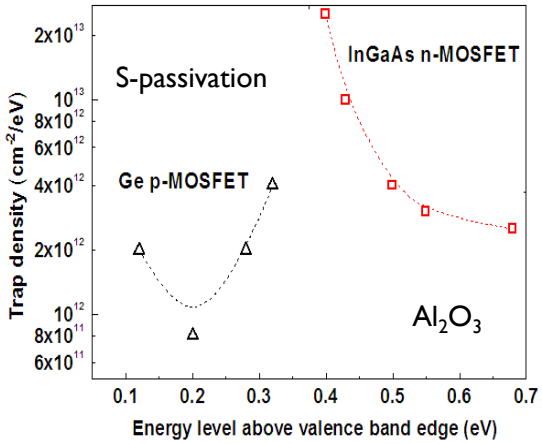
- A wide range of materials could be grown on a Silicon wafer with Ge as an intermediate material to achieve low defect-density III-V Silicon
  - Most interesting candidates: GaAs, InGaAs, InAs, …..

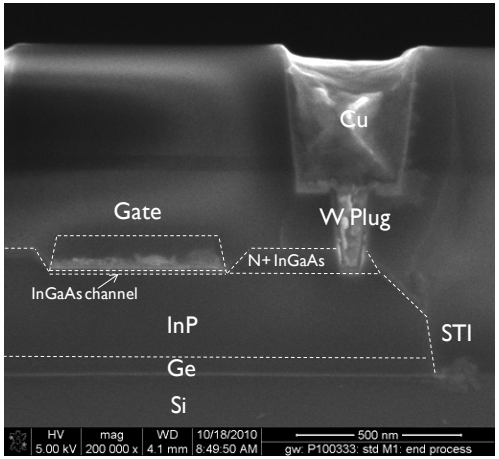
HIGH-MOBILITY IIIV-BASED QW DEVICES

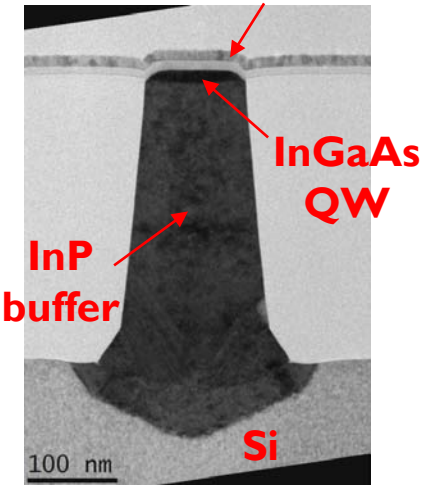
[Imec, IEDM'09]







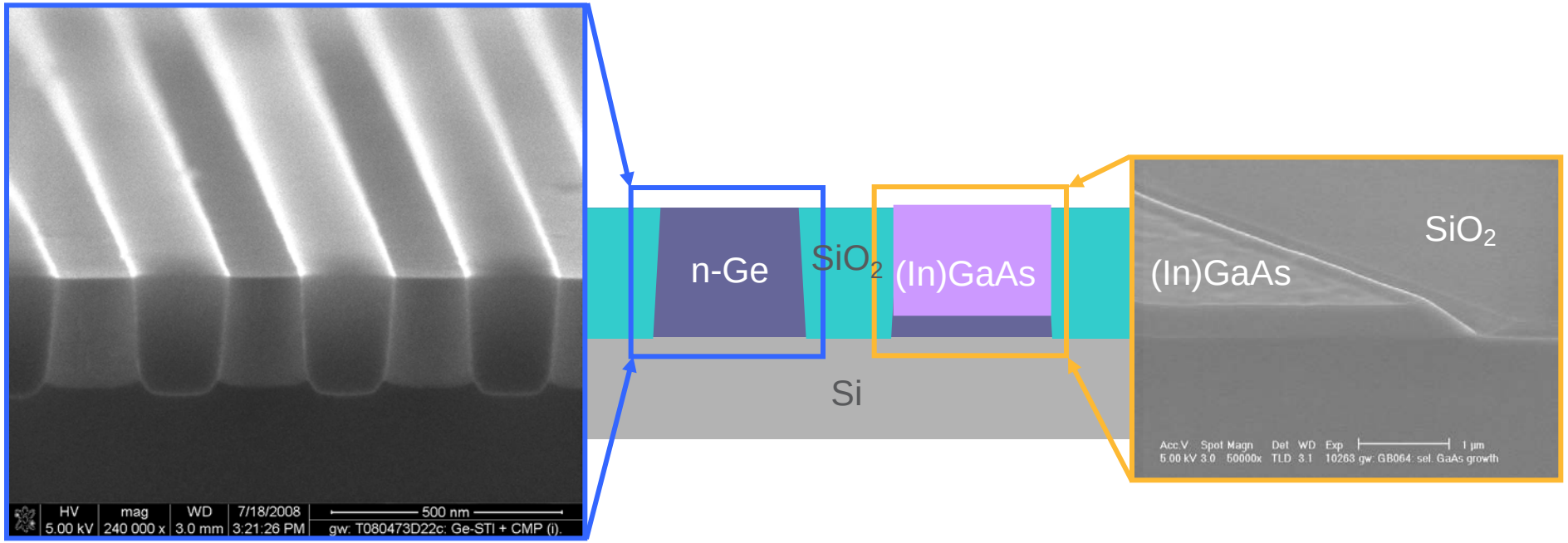




- Demonstration of:
  - ✓ Common gate stack for IIIV & Ge based devices
  - ✓ Selective IIIV integration, directly on Silicon substrate
- Issue left of Dit @ interface IIIV – gate stack

SELECTIVE EPI GROWTH OF Ge AND III/V AFTER STI

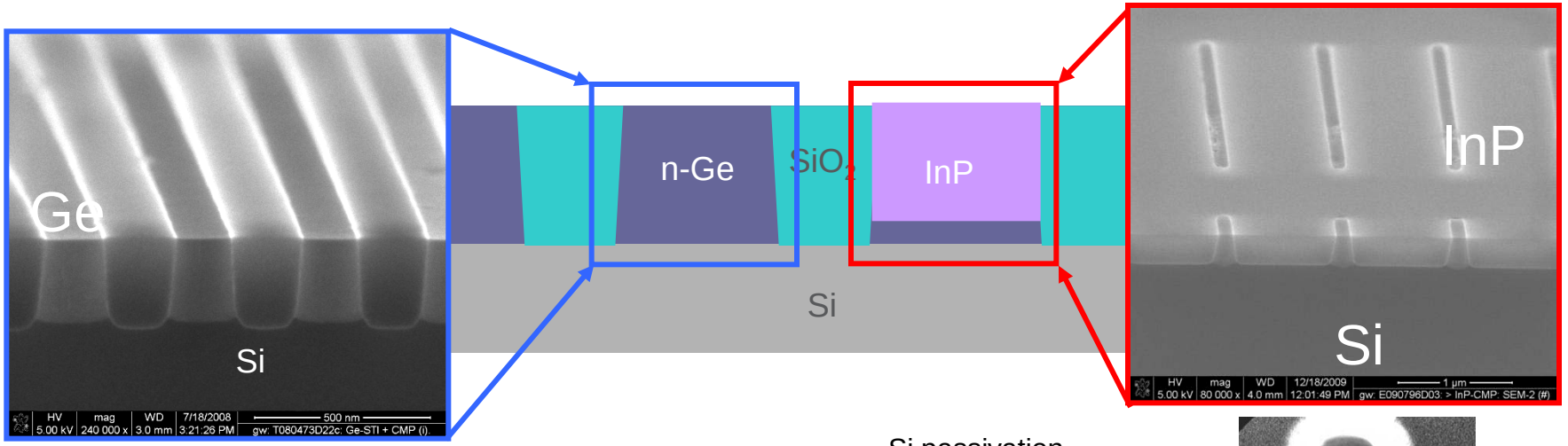
- Selective growth of Ge epi after STI formation on Si wafer
  - Low defect densities obtained after proper annealing
  - Provides flat surface that allows further scaling of transistor gate length

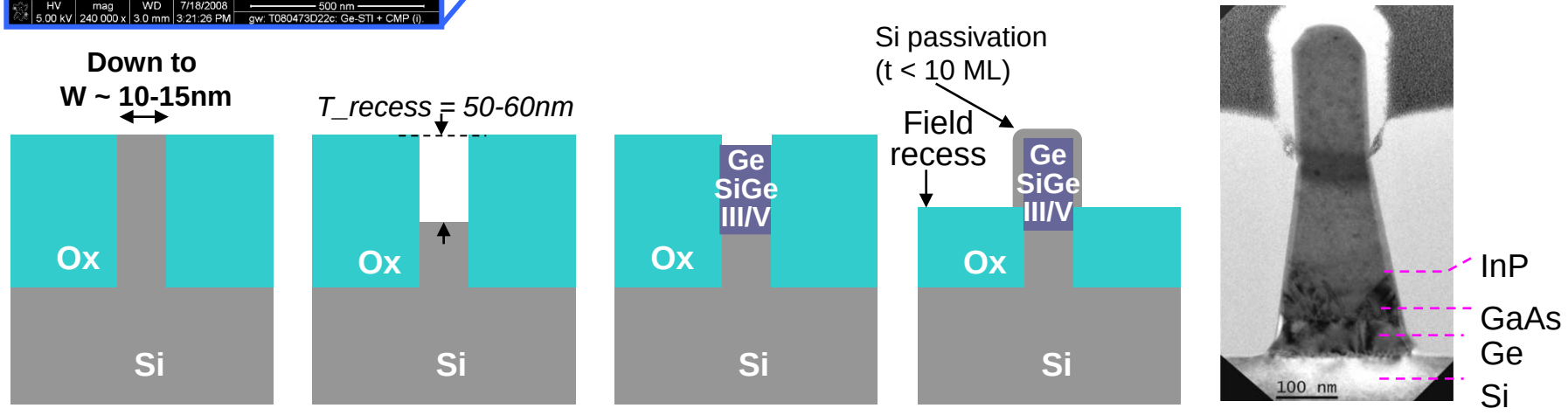


- Good quality selective growth of thin (In)GaAs on Ge demonstrated
  - No large defects or dislocations can be observed by TEM

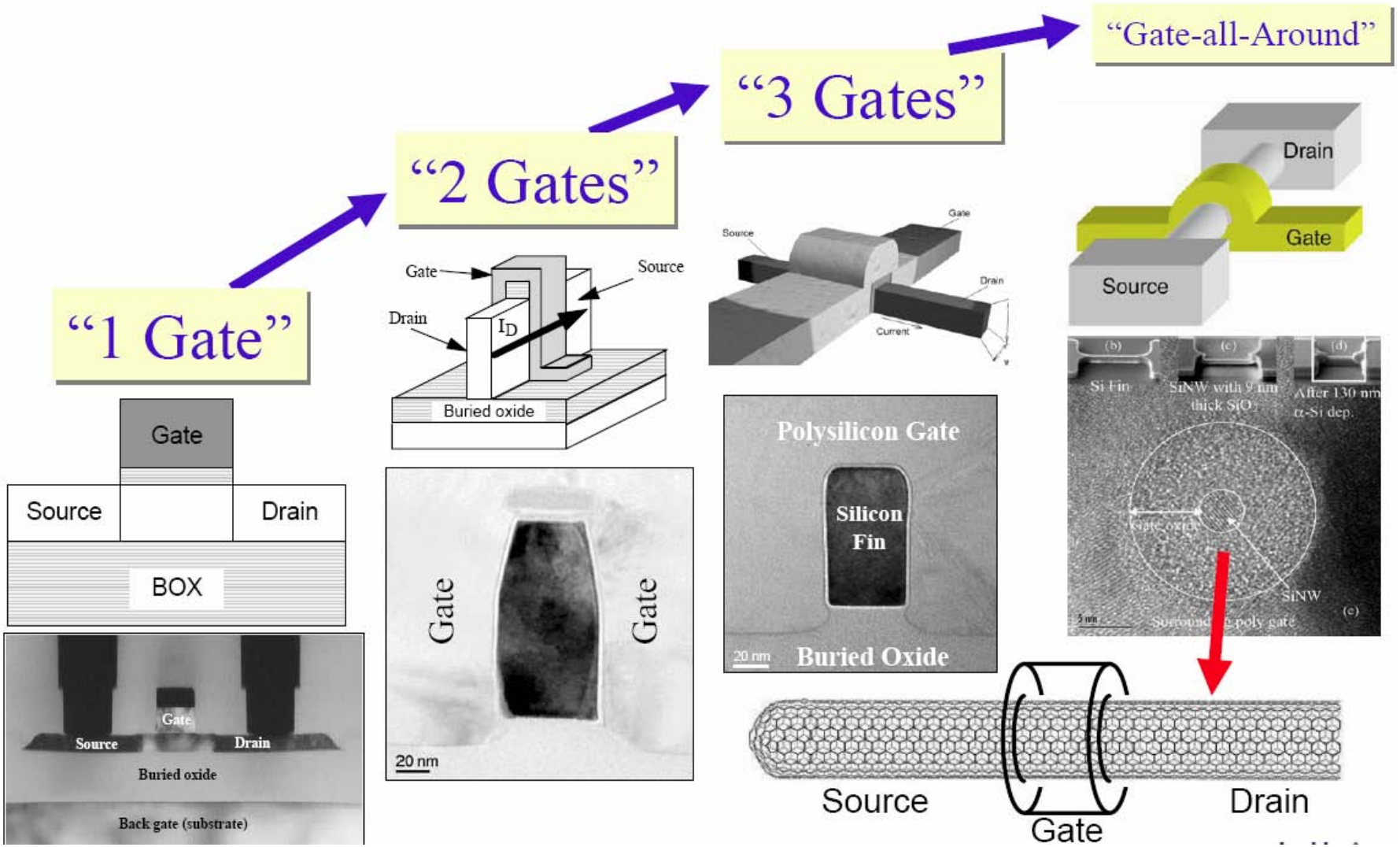
SELECTIVE GROWTH OF Ge AND III/V ON SI WAFERS

- ☑ Local selective growth after STI allows integration of Ge and III/V materials on Si wafers, also for FinFET's.
  - **confined growth to grow materials with high lattice mismatch to Si, >> t_c**

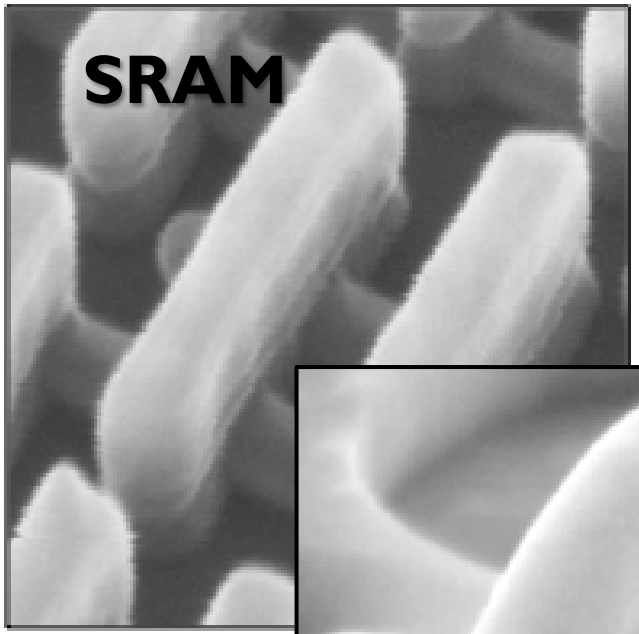


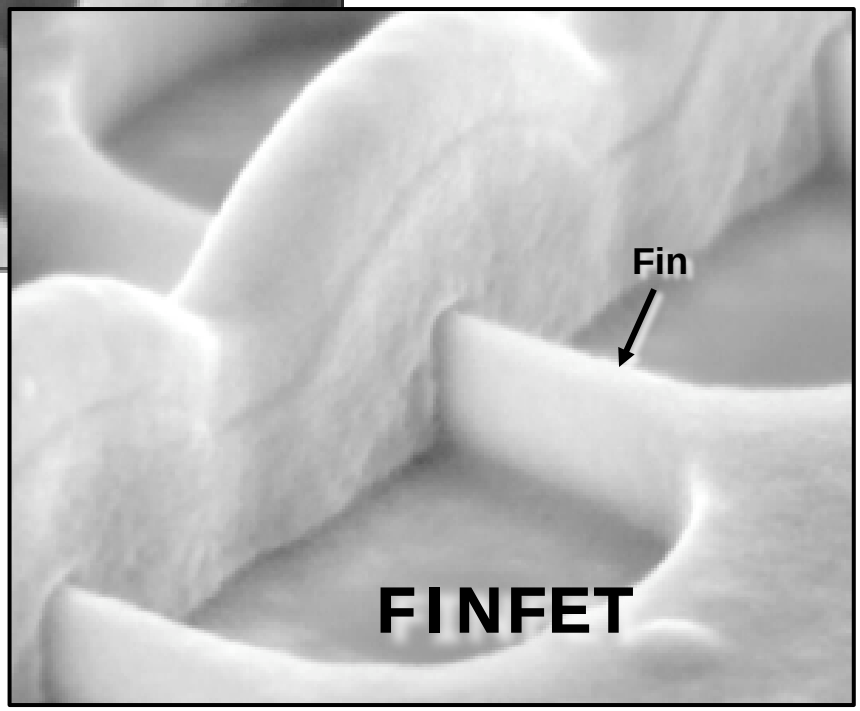


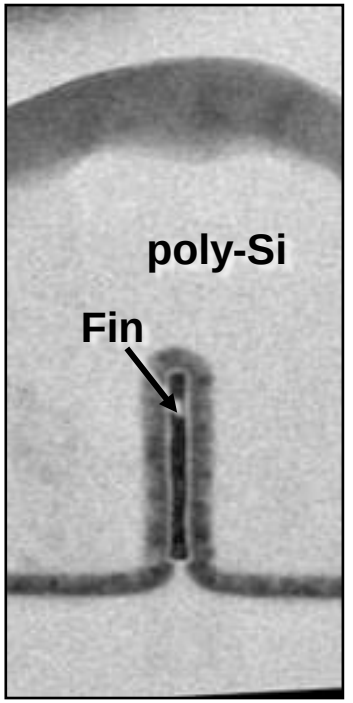
MULTI-GATE STRUCTURES



MATERIALS AND DEVICES

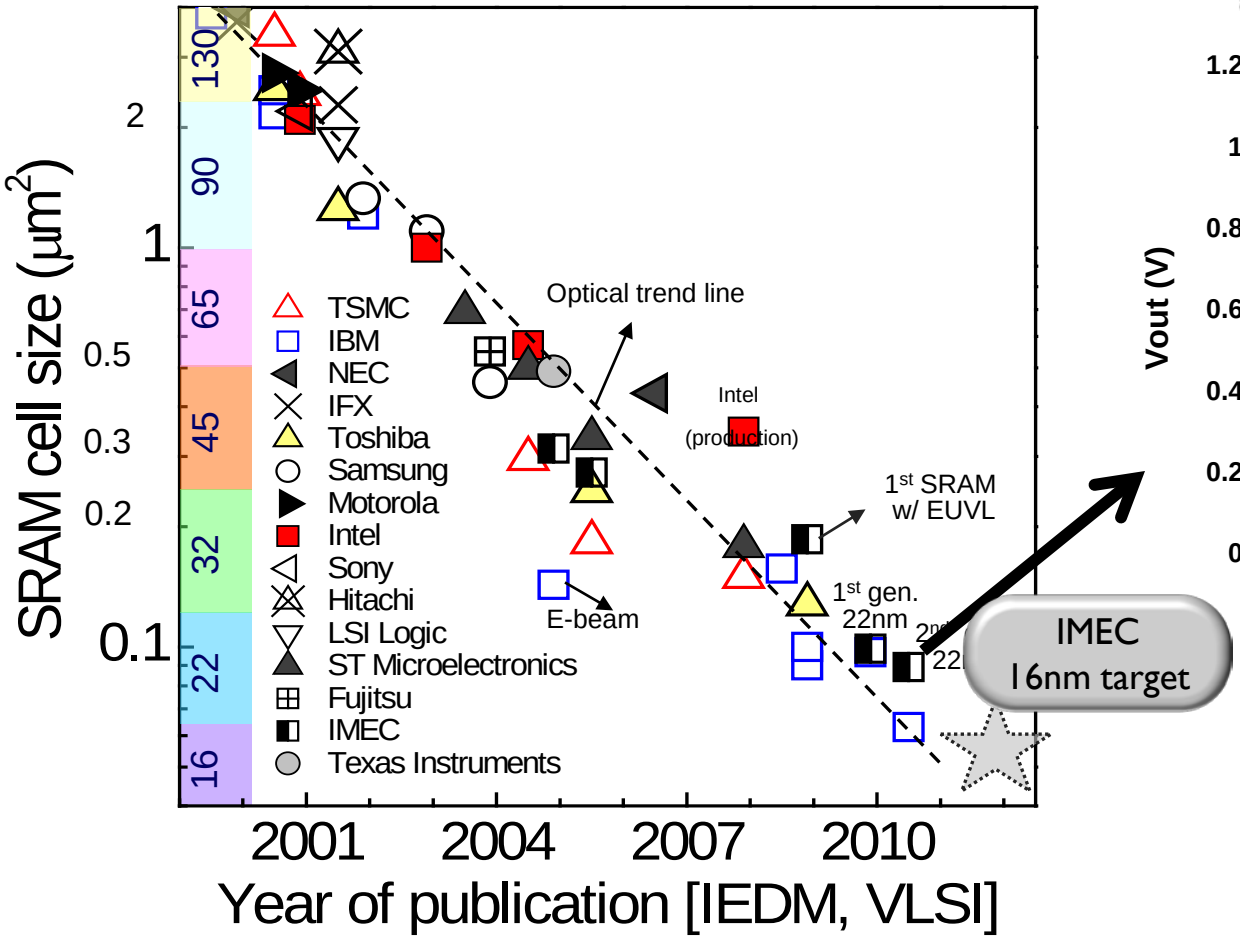






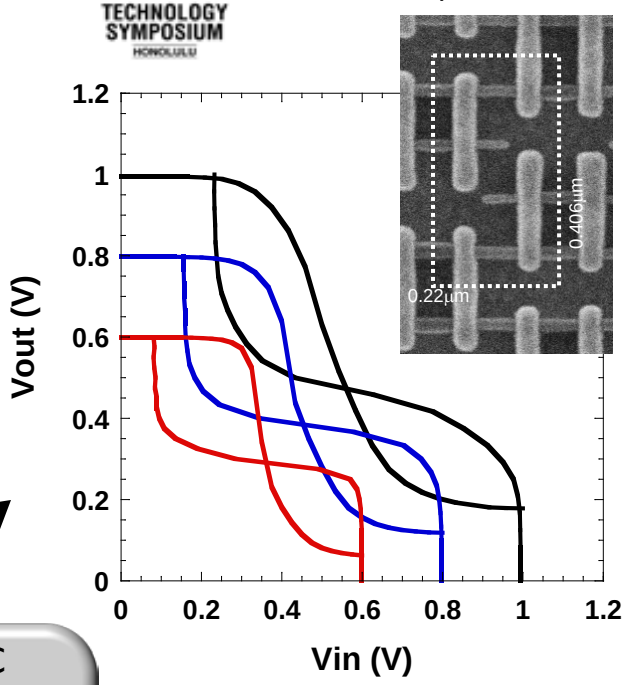
Strained Si
High-k
Metal gate
Multi gate

SRAM CELL SIZE ROADMAP



2010 VLSI TECHNOLOGY SYMPOSIUM HONOLULU

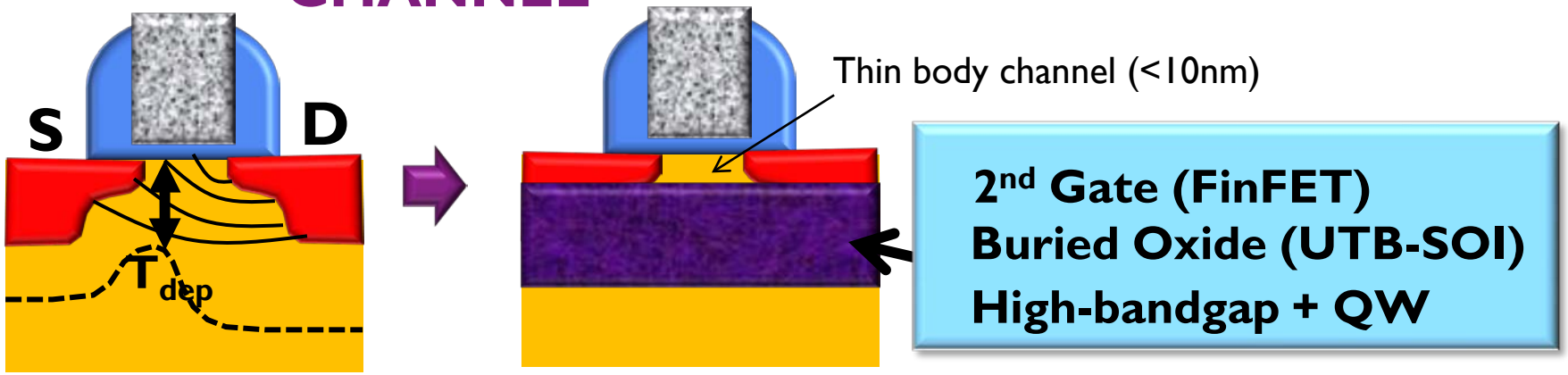
0.089μm² SRAM

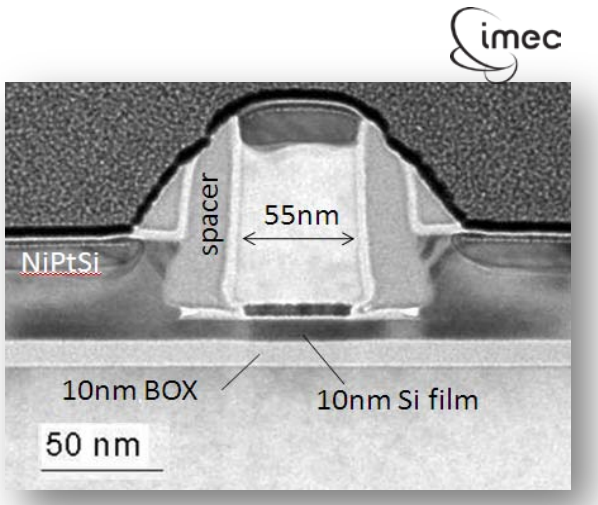


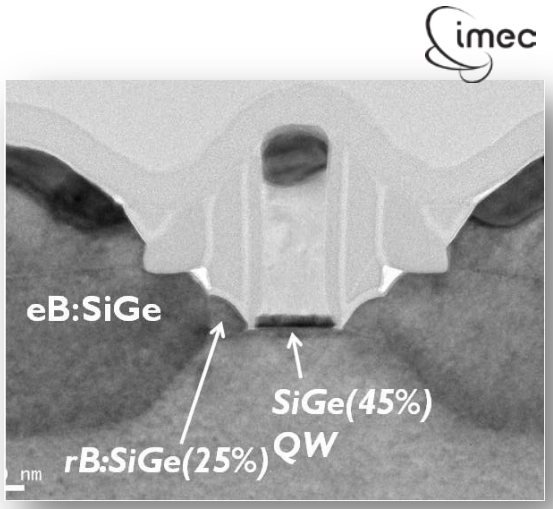
Single → Double patterning

- ✓ 2nd generation FinFET-based 22nm SRAM cell (10% smaller)
- ✓ *... and already gearing for 16nm!*

CONCEPTS FOR FULLY DEPLETED CHANNEL

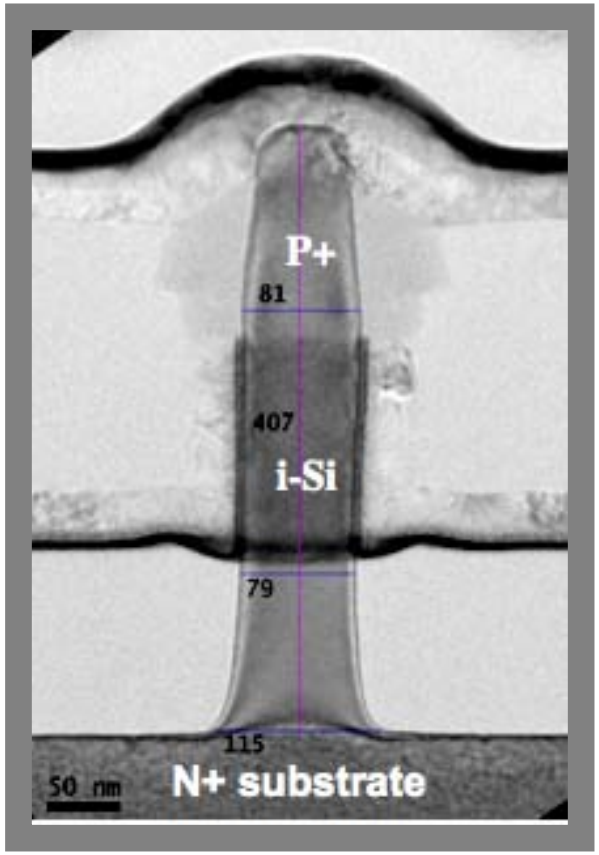




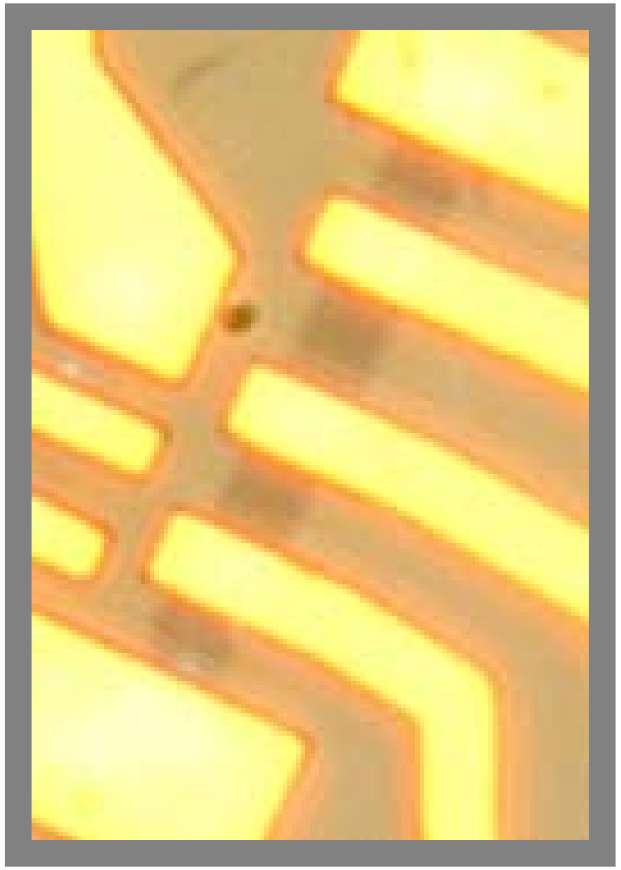


FinFET | **UTBox-SOI** | **Quantum Well**

EXPLORATORY CONCEPTS



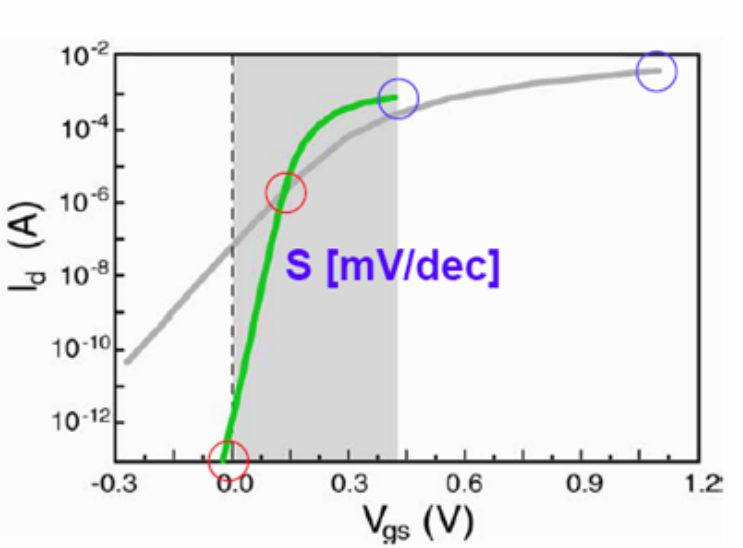
Tunnel FET

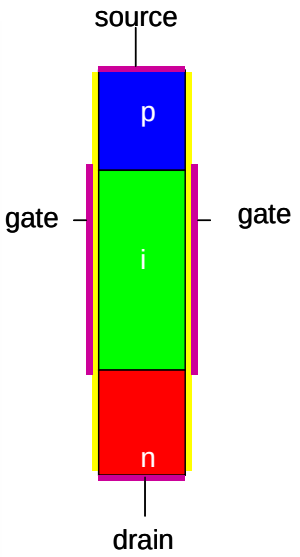


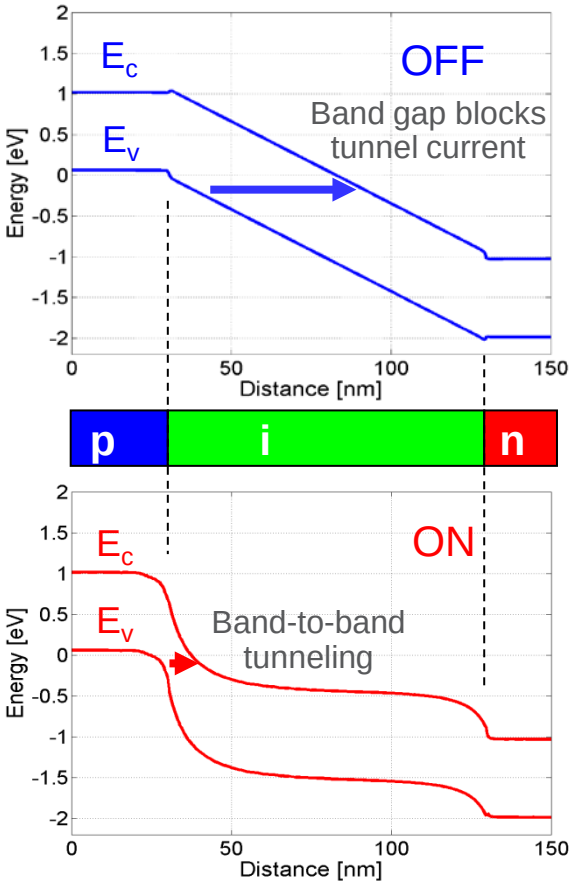
Graphene FET

DEVICES WITH REDUCED POWER CONSUMPTION

- **Improved subthreshold slope devices can have high I_{ON}/I_{OFF} ratio at low switching voltage → reduced supply voltage and power consumption**
  - For carrier transport limited by thermionic emission over a barrier: $d\psi_S/d(\log_{10}I) \approx 60$ mV/decade at room temperature







- **TunnelFET basic idea: *use the band-to-band tunneling as an energy filter to overcome the 60mV/decade subthreshold slope limitation***
  - ON/OFF switching determined by band-to-band tunneling at source side

CHOICE TFET MATERIAL: EFFECT OF BANDGAP

- tunneling probability ~ $(E^2 m_r^{1/2} . E_g^{-0.5})$ $\exp(-A . E_g^{1.5})$

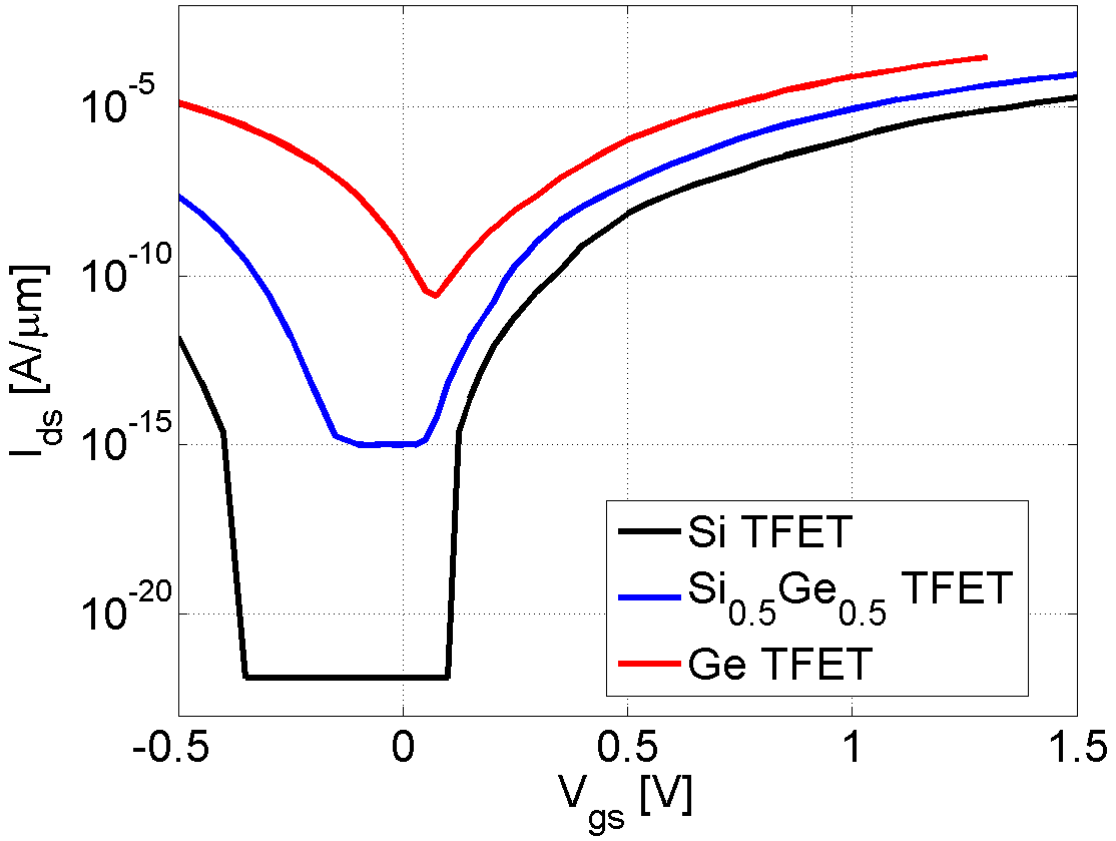
$E_{g,Si}$ = 1.12 eV

$E_{g,Ge}$ = 0.66 eV

- *I-V* curves show:

$I_{ds,Ge} \approx 100\ I_{ds,Si}$

- smaller bandgap improves tunneling, but want silicon-based

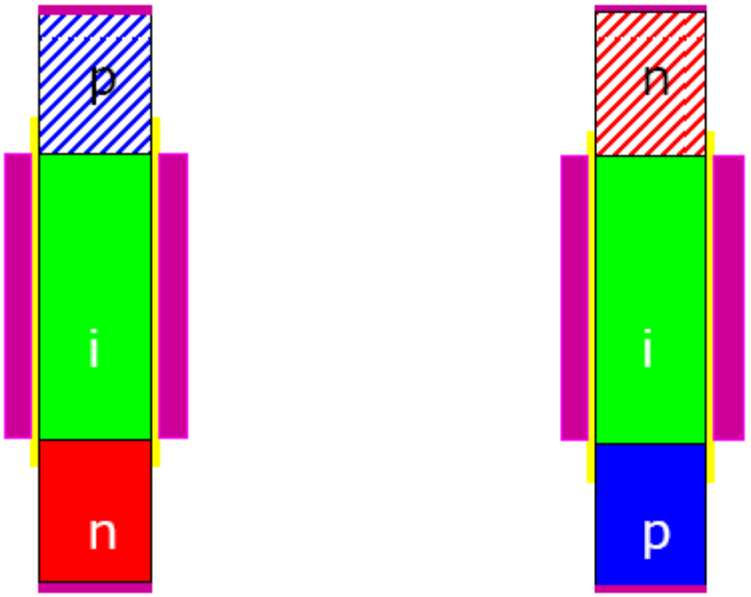


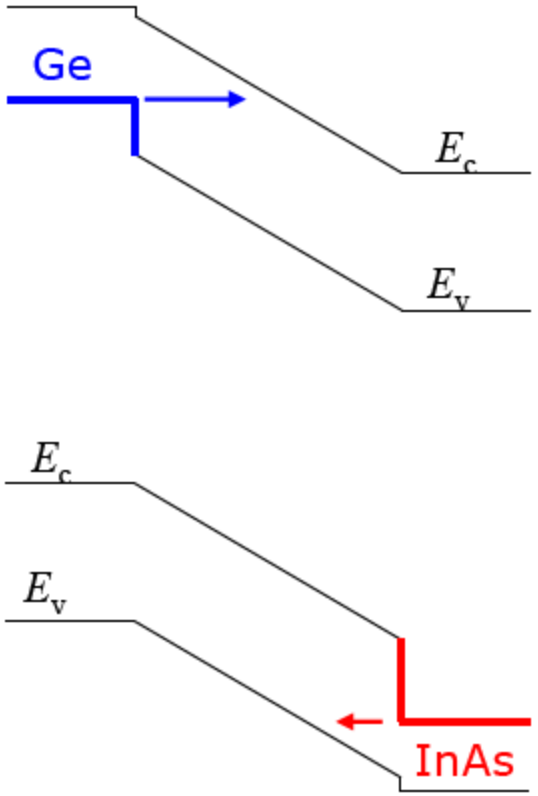
Remark: Ge TFET-curve is shifted to the left for easier comparison

COMPLEMENTARY HETERO-STRUCTURE TFETS

Ge-source n-TFET

InAs ($In_{0.6}Ga_{0.4}As$) -source p-TFET





: silicon

: germanium

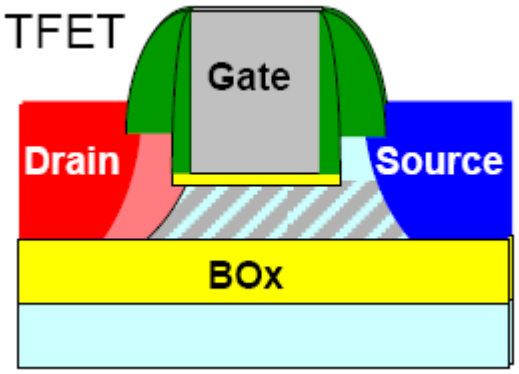
: indium-arsenide

V_{DD} ~ 0.25V ("Green" Transistor)

A. Verhulst et al., IEEE Electron Dev. Lett., 29, 1398 (2008)

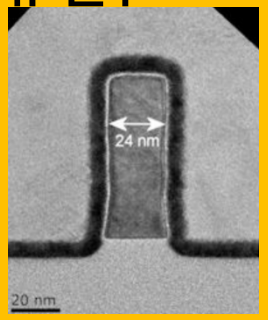
Literature

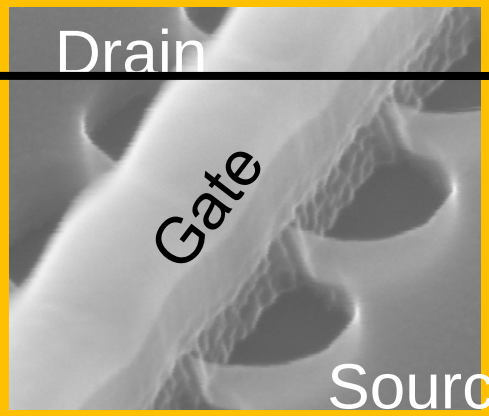
Horizontal



Mayer *et al.*, IEDM (2008)

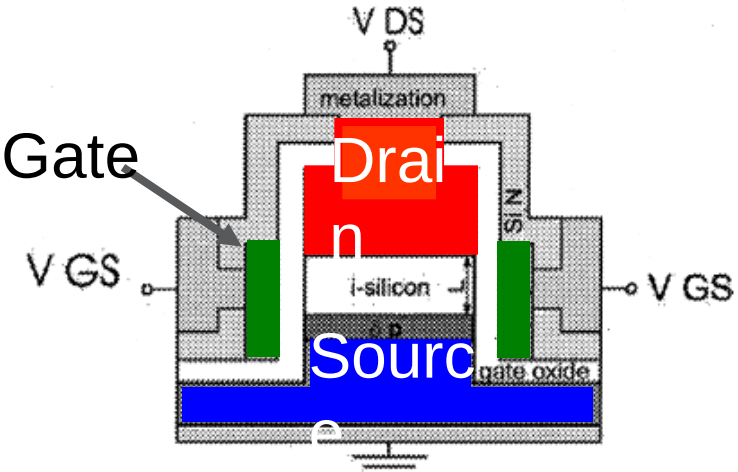
FinFET





Leonelli *et al.*, *SSDM* (2009)

Vertical

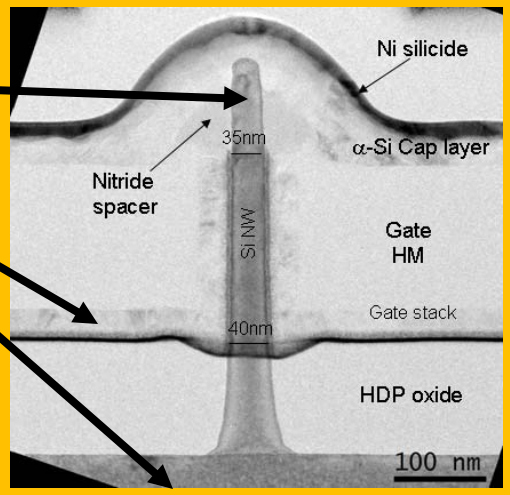


Bhuwulka *et al.*, IEEE TED(2004)

Nanowires Source

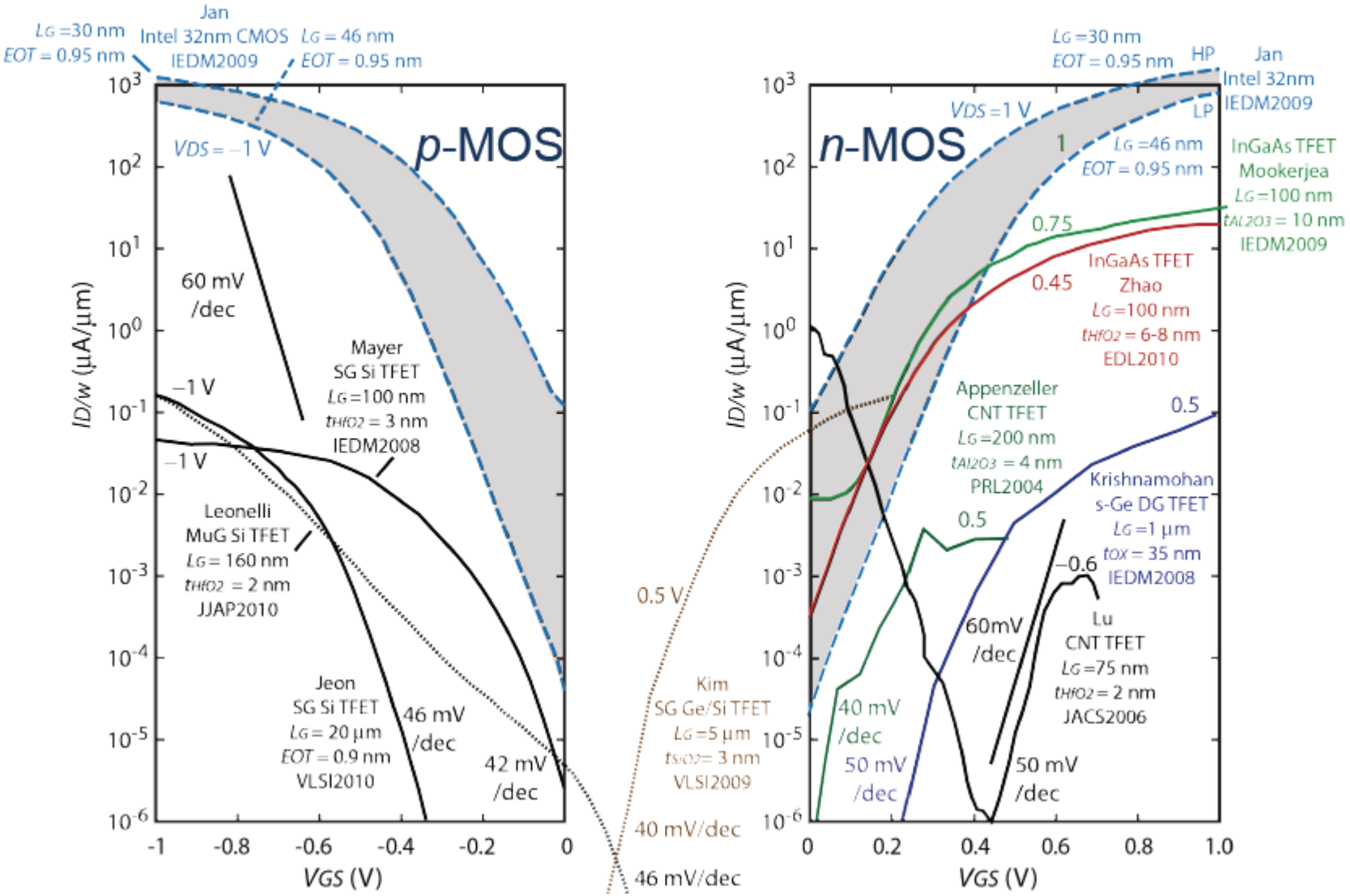
Gate

Drain



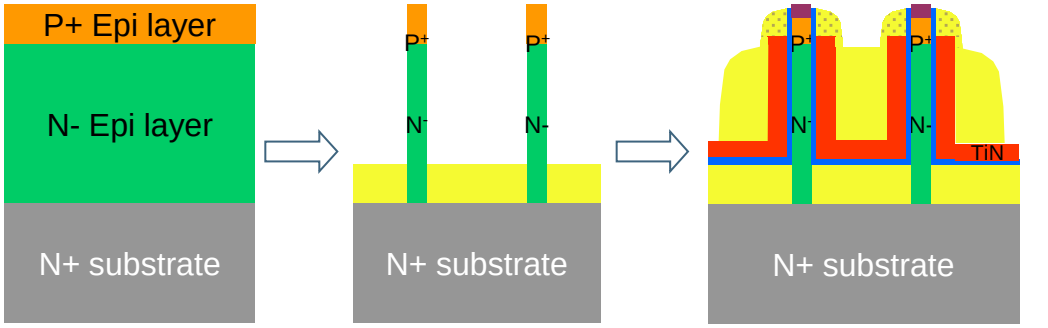
Vandooren *et al.* VLSI Workshop (2009)

TFET PERFORMANCE SUMMARY - SEABAUGH

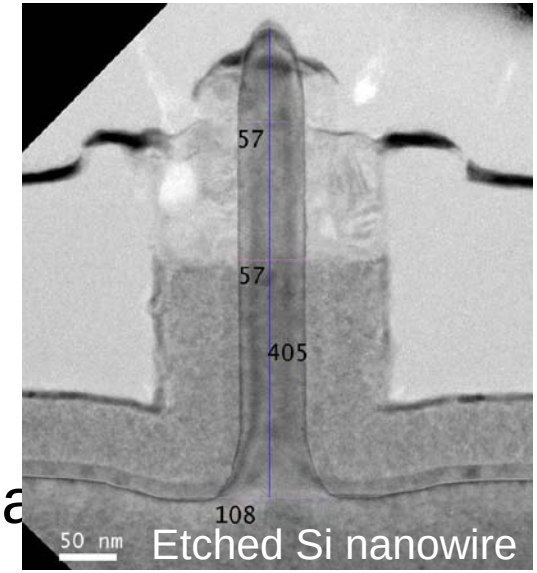


TUNNEL FET BASED ON NANOWIRES

- Possible implementation of Tunnel FETs using etched nanowires

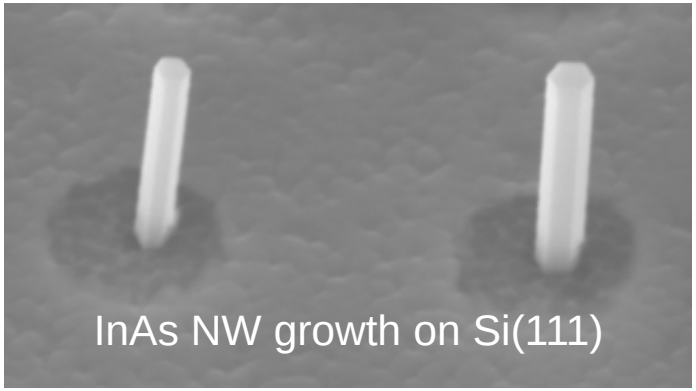


etched nanowires TFET implementation

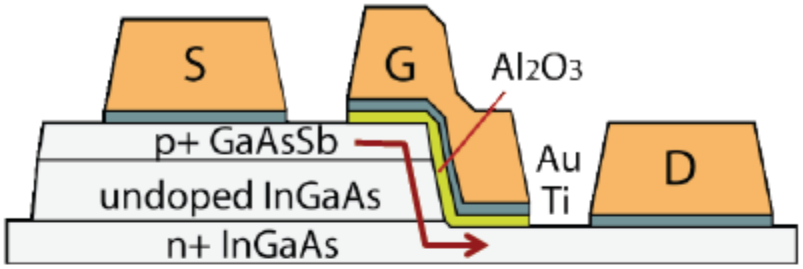


- Templated and constrained growth of na

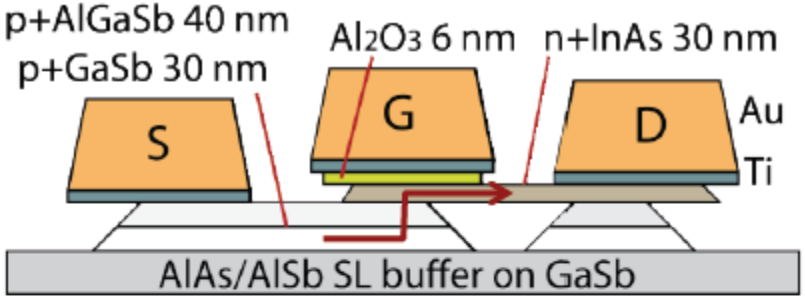
Growth can be performed partially or fully constrained, with or without catalyst



III-V AND GRAPHENE TFETS

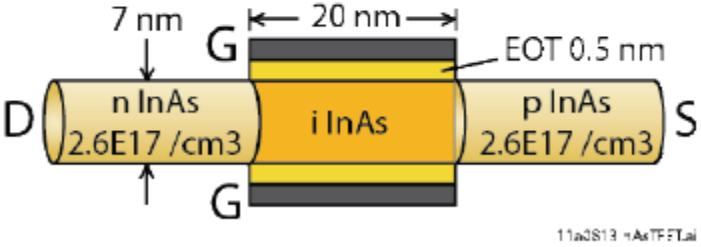


tunneling // to the gate
oblique to the gate field

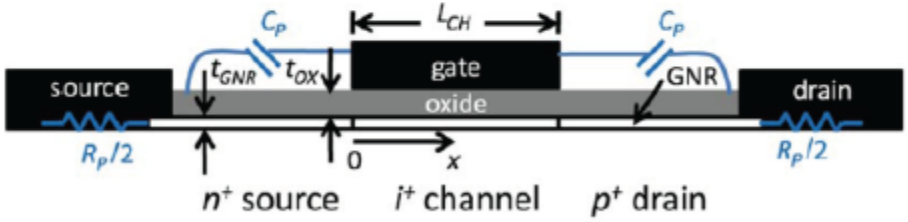


tunneling ⊥ to the gate
in-line with the gate field

Tunnel transistors geometries



nanowire TFET
gate-all-around - best electrostatics

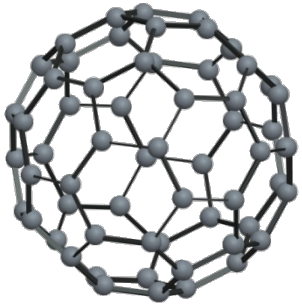


graphene nanoribbon (GNR) TFET
n an *p* channel currents commensurate

A. Seabaugh – ESSDERC 2011

CARBON STRUCTURES

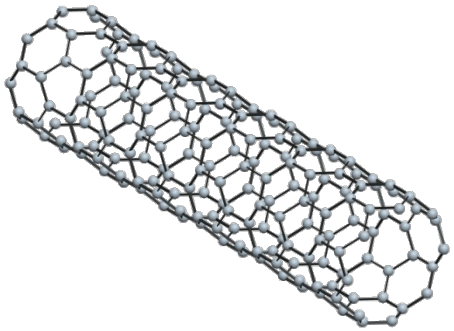
0D



Fullerenes

Curl, Kroto &
Smalley 1985
Nobel prize 1996

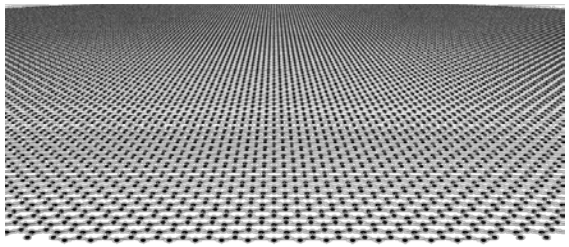
1D



Carbon nanotubes

Multi-wall 1991
Single-wall 1993

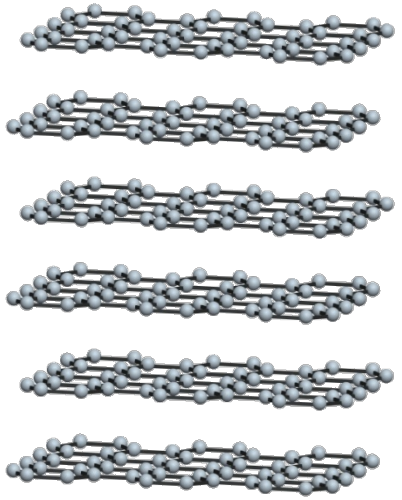
2D



Graphene

2004
Geim, Novoselov
Nobel prize 2010

3D

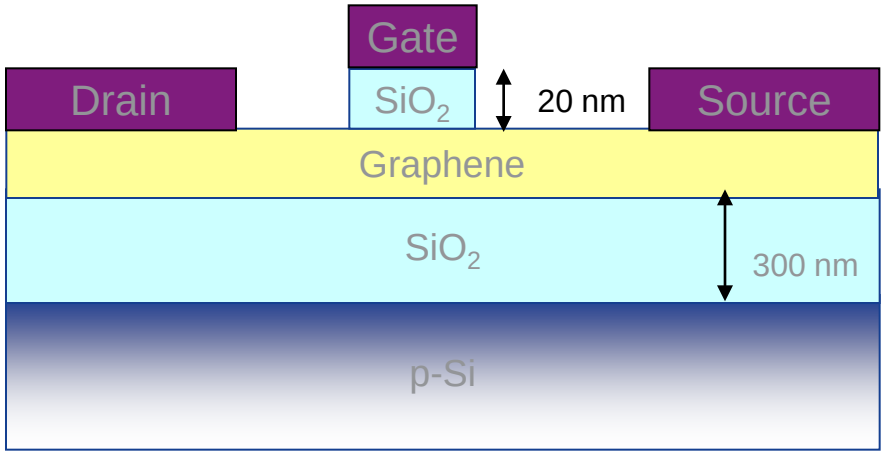


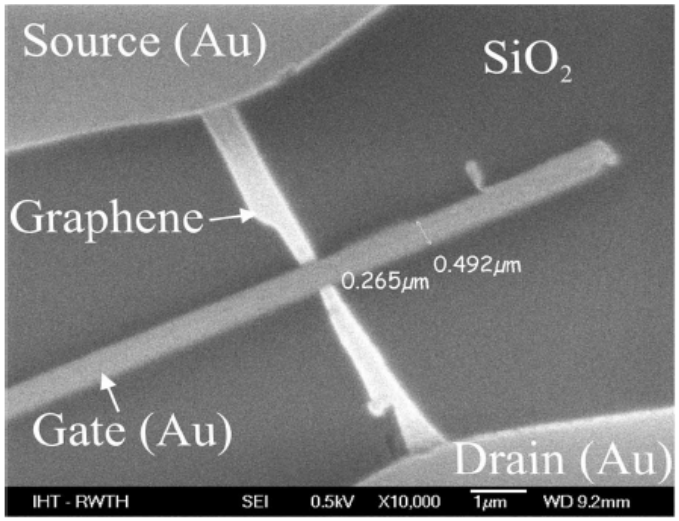
Graphite

XVI century

FIELD-EFFECT DEVICES

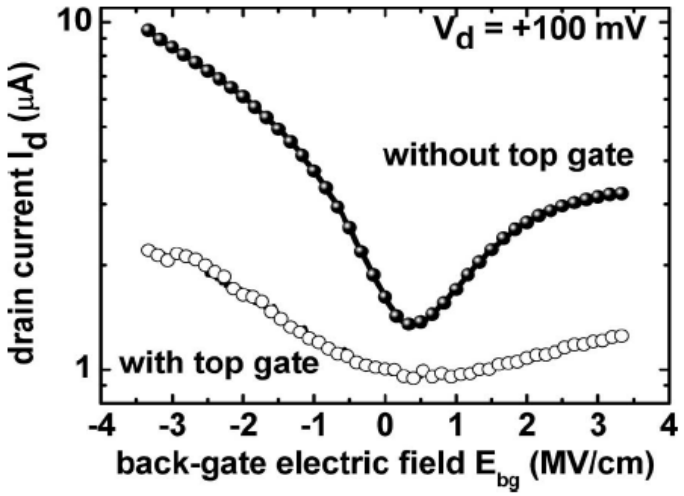
"Classical" field-effect approach





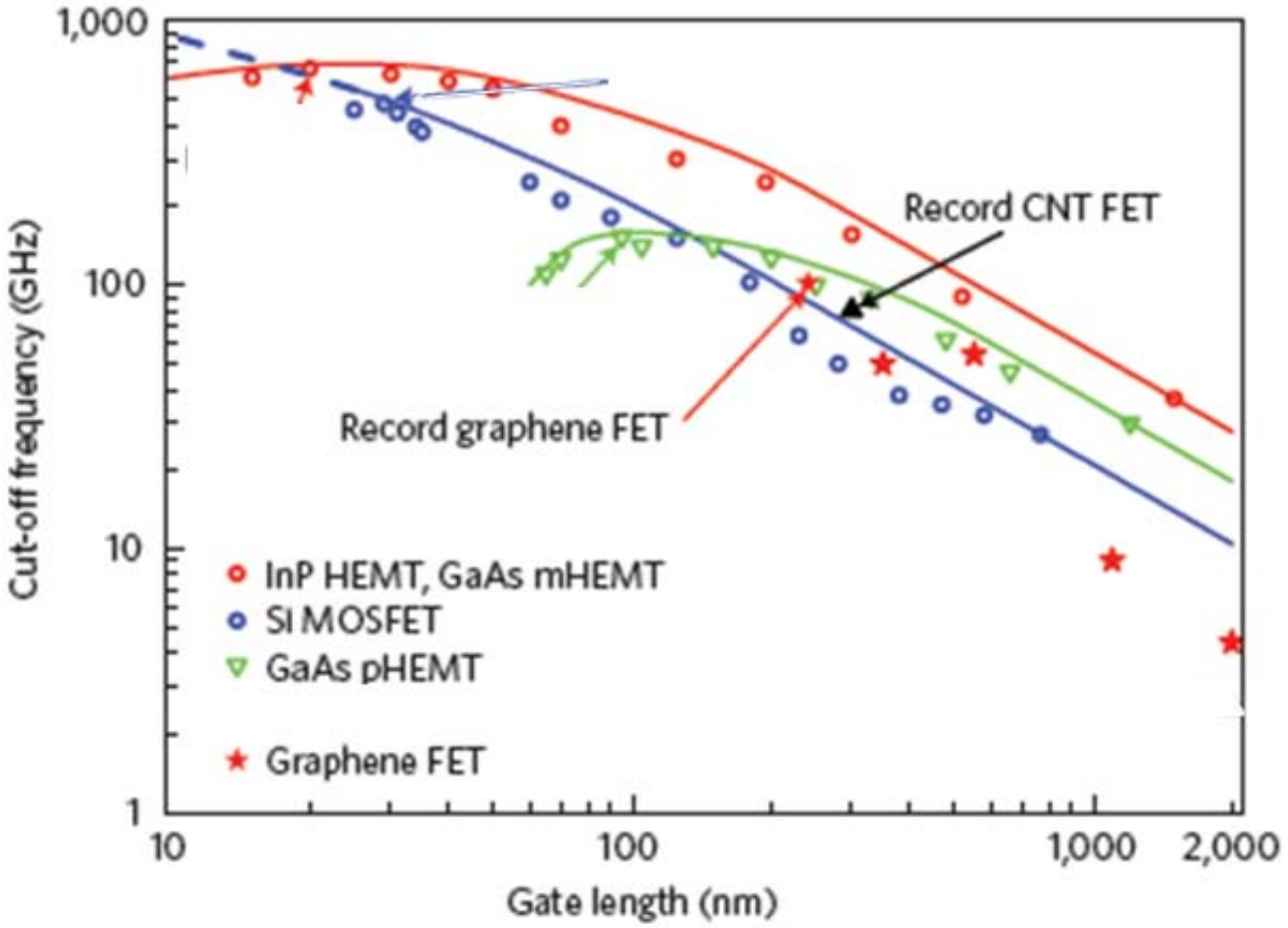
- Top and bottom gates
- Ion/Ioff ratio ~10 at 300K

Cannot switch it off!



Lemme et al., IEEE Electron. Dev. Lett. ***28****, 4 (2007)*

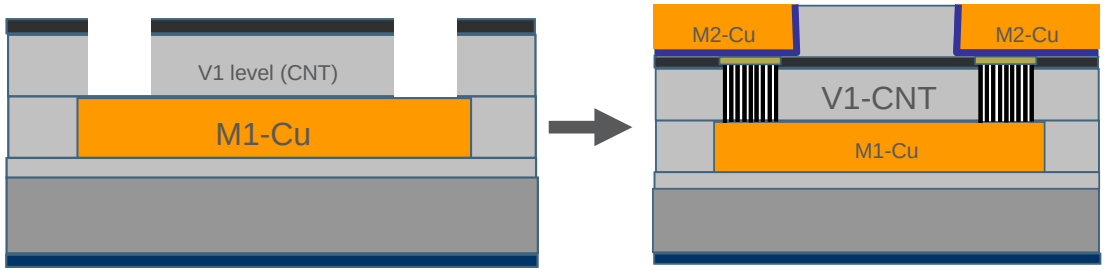
COMPARISON OF FREQUENCY PERFORMANCE



F. Schwierz, Proc. Int. Conf. on Solid-State and Integrated Circuit Techn., Eds. T.-A. Tang and Y.-L. Jiang , pp. 1202-1205 (2010)

CNT INTERCONNECTS

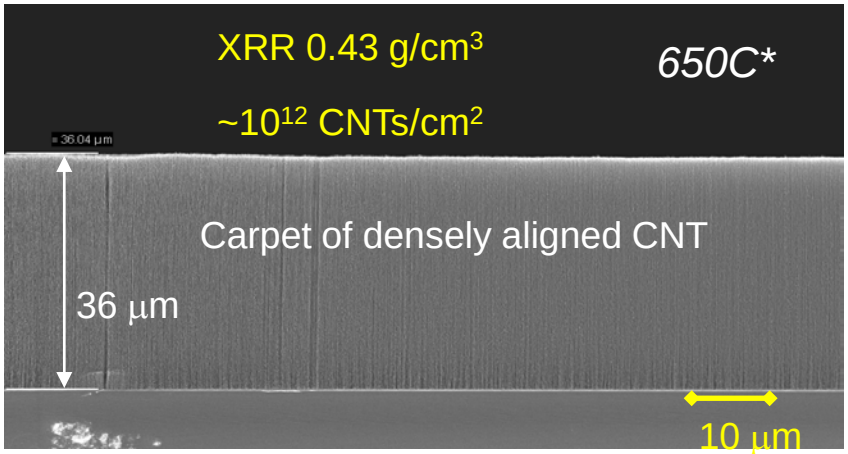
- CNT exhibit enhanced electrical and thermal properties over Cu

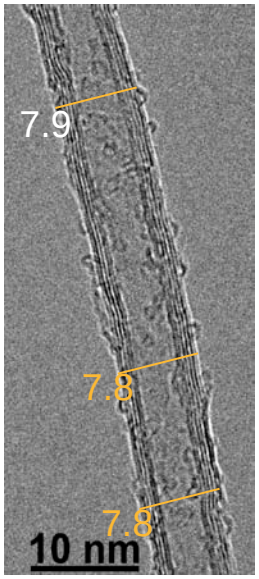


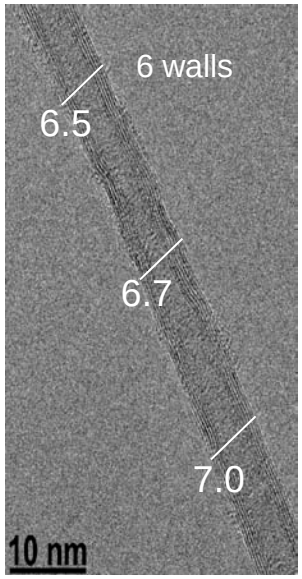
Current capacity:
- Cu ~ 10^6 A/cm^2
- CNTs ~ 10^9 A/cm^2

Thermal conductivity:
- Cu ~ 400 W/m·K
- CNTs ~ 5000 W/m·K

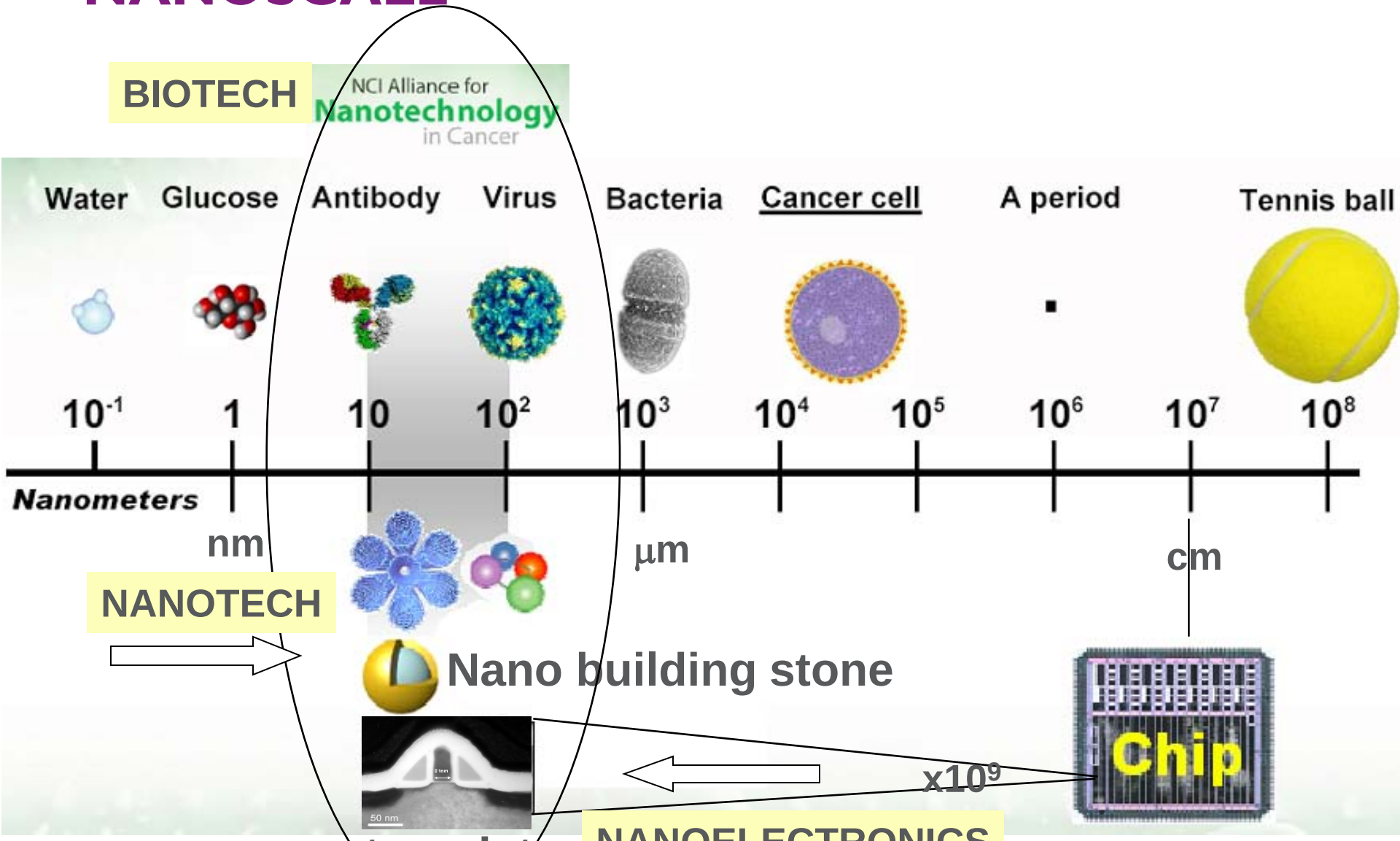
- High-density of MW CNT obtained with Fe on Ti
  - Approaches density needed for interconnects ~10^{12} MWCNT or ~10^{13} cm^{-2} CNT shells
    - Outer diameter of 6.5 – 8.0 nm (with 7- 10 sheets), inner diameter ~ 5nm



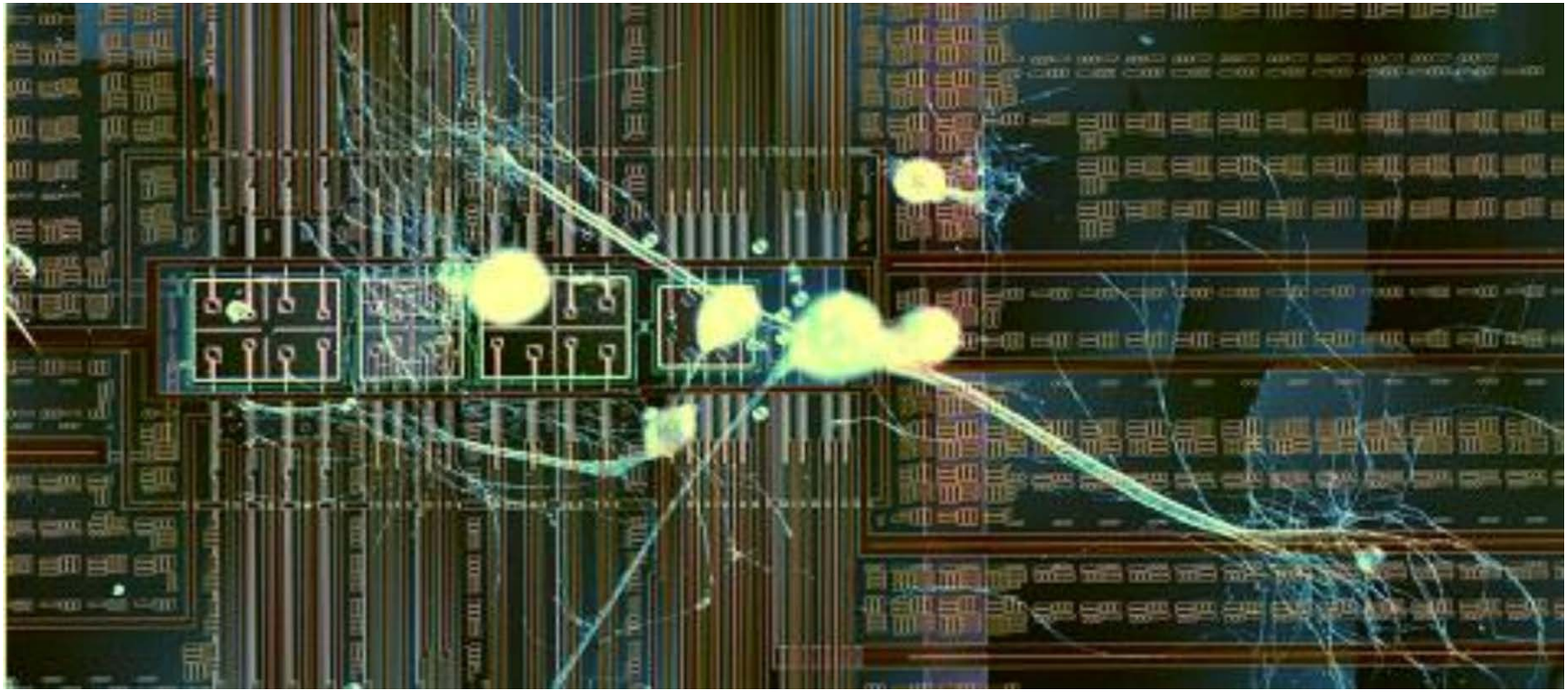




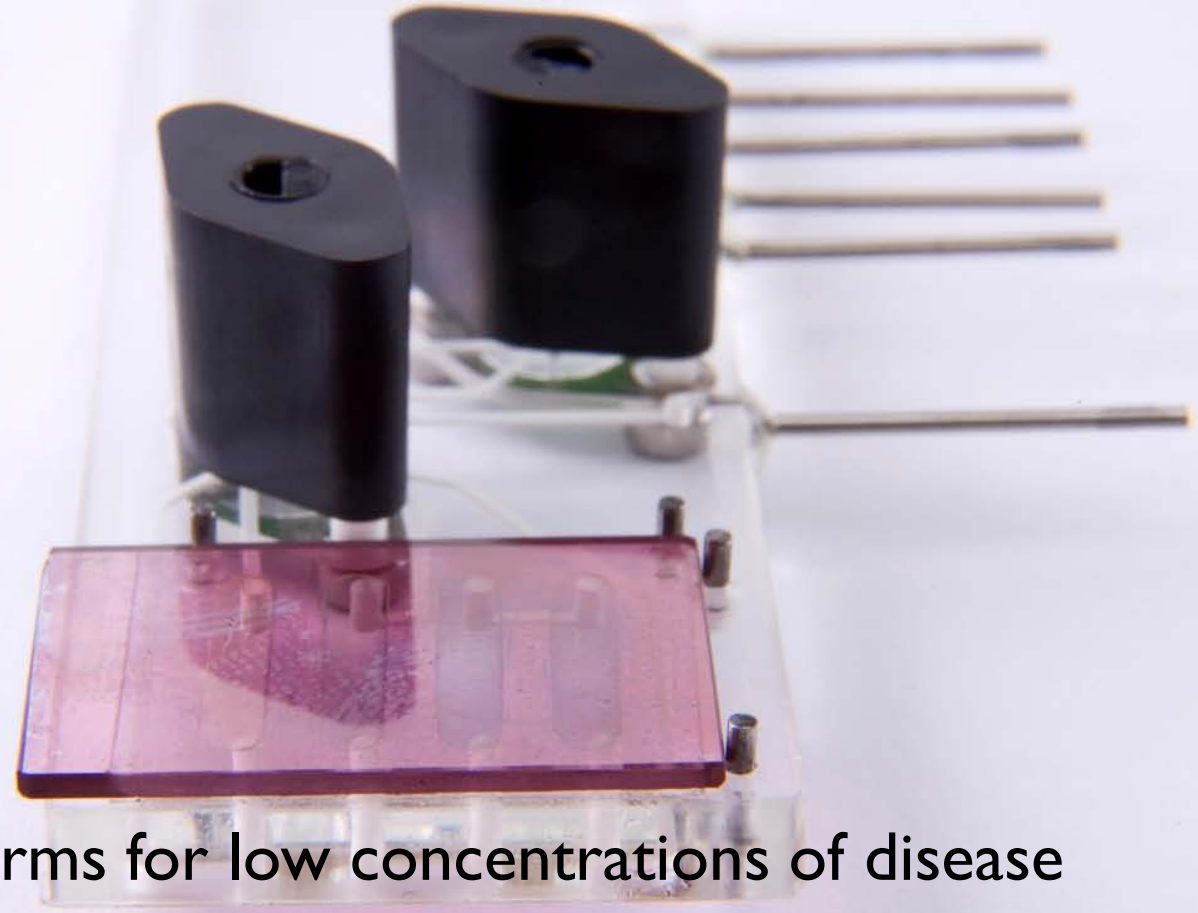
NANO-BIO VISION: BIO AND ICT MEET AT THE NANOSCALE



ARTIFICIAL SYNAPSE = functional interface allowing bi-directional communication between a neuron and an integrated circuit = neurons-on-chip

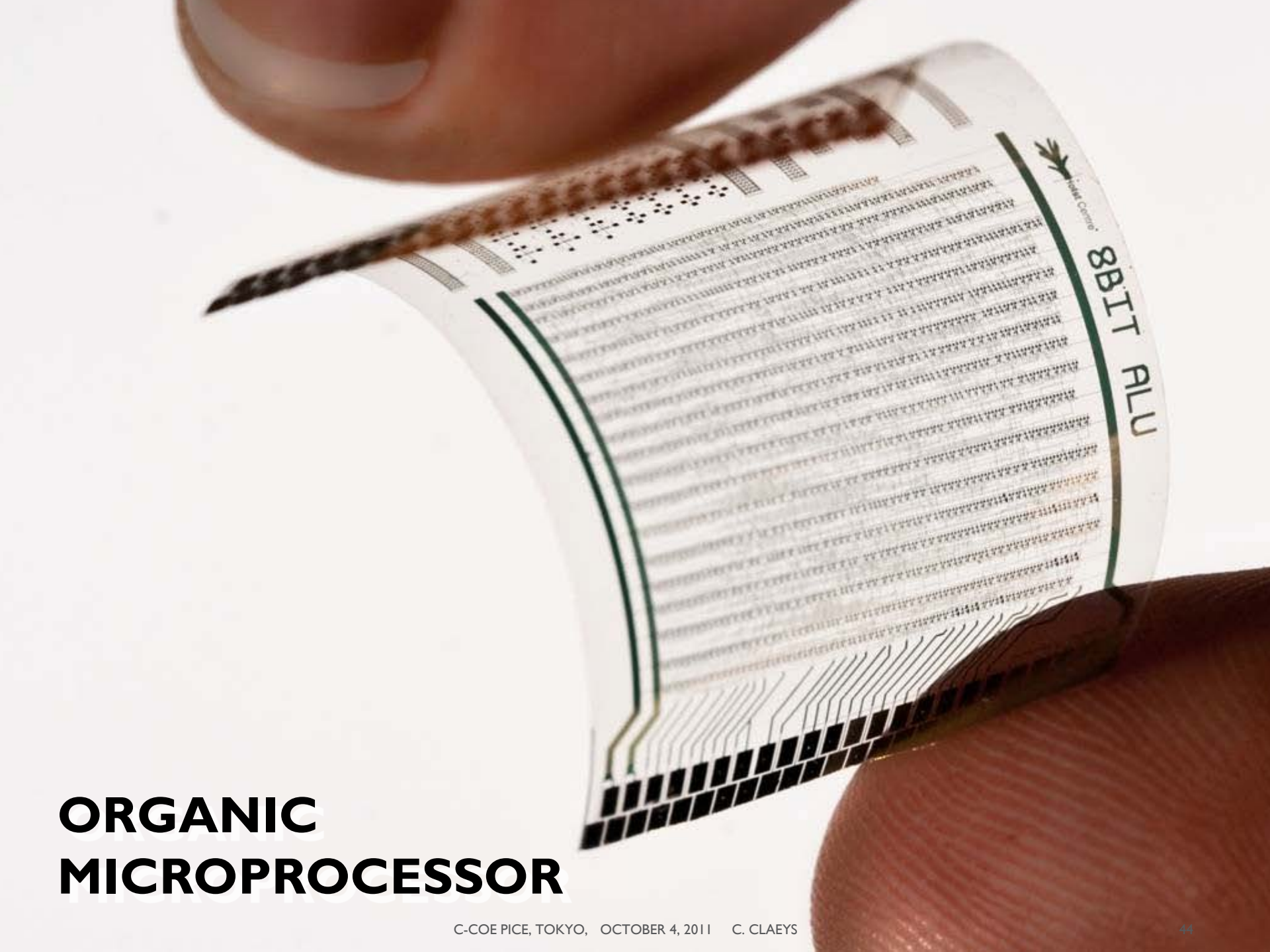


A MEDICAL LAB OF ONLY 1X1 cm^2

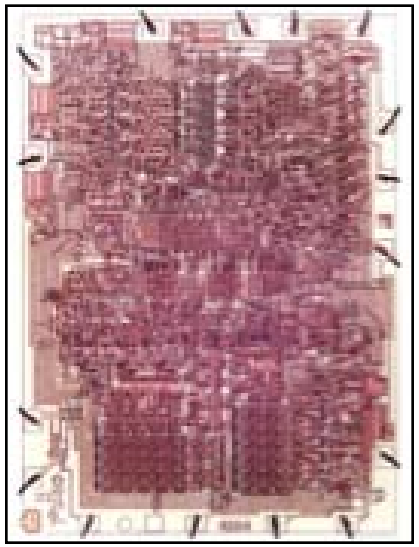


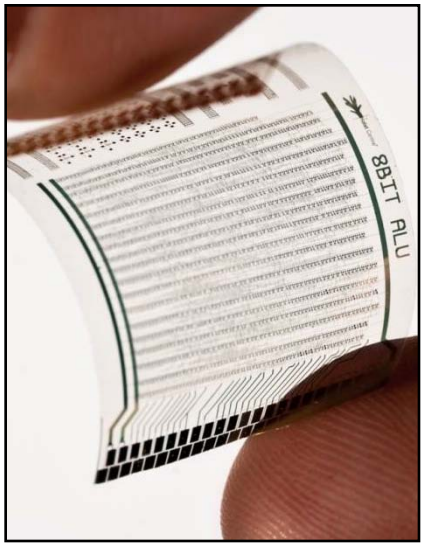
Detection platforms for low concentrations of disease molecules:

- Fast
- Easy to use
- Cost effective



ORGANIC MICROPROCESSOR





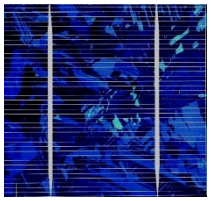
1971: Intel 4004	2011: imec & Holst
First Si µProc.	First plastic µProc.
10 µm	5 µm
4 bit	8 bit
pMOS	pMOS, dual Vt
-15V Vdd	-10V Vdd
2300 TOR	2000 TOR
108 KHz	6 Hz

Courtesy P. Heremans

SOLAR+ Roadmap

Thick(>180µm) bulk Si

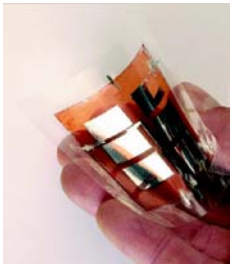
Single X ⇒ Multi X



Thin-film c-Si < 20 µm

Epitaxial cells
Cells on ceramic/glass

Fully organic Thin-film cells for large-scale power generation



Organic cells for consumer applications

Achievable direct cost module level (€/W_p)

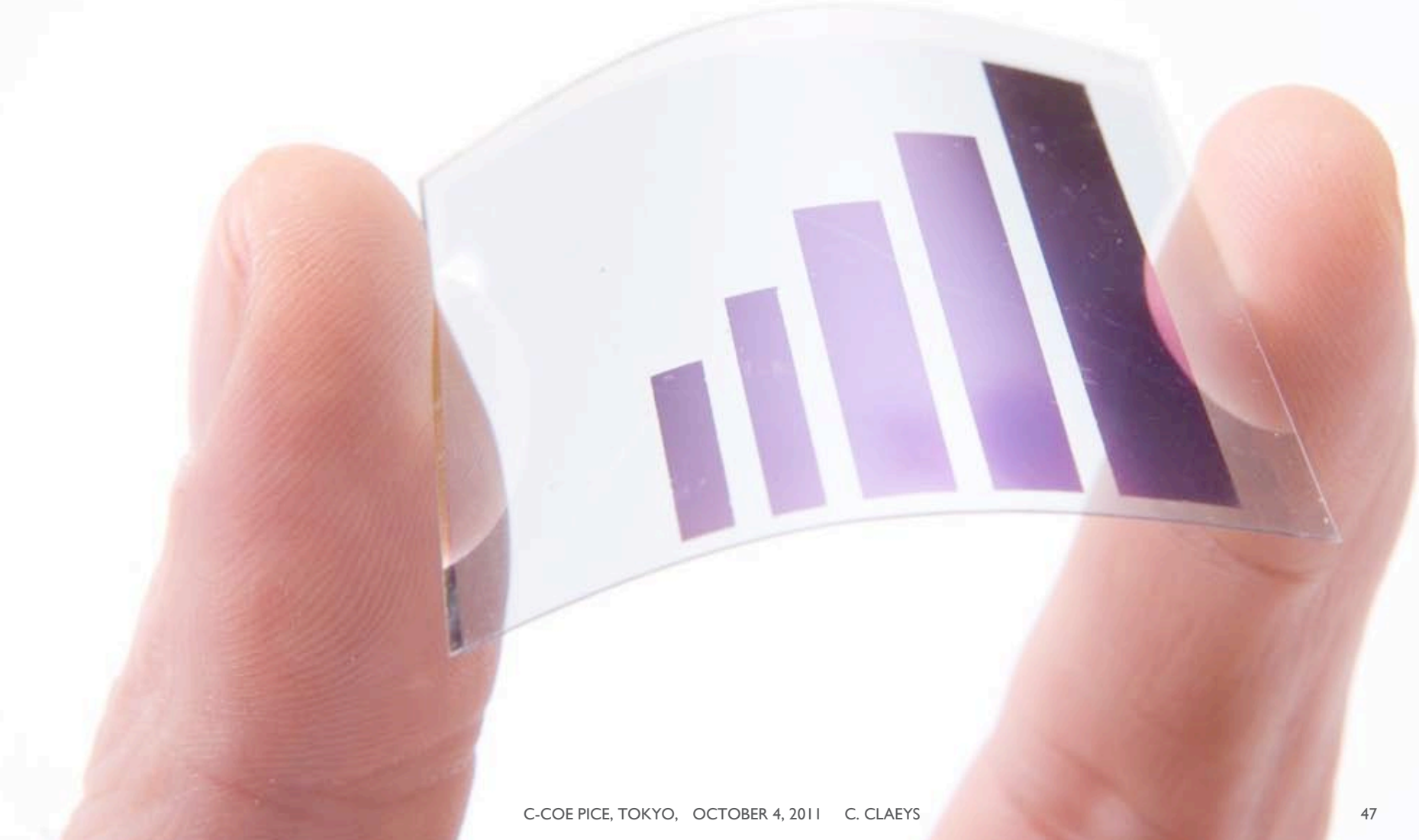
2.7-3.5	1.3-1.5	1.1-1.3	0.5-1.0	< 0.5
300µm multi	150µm multi	Thin ribbon	Thin-film	Organic cells

t

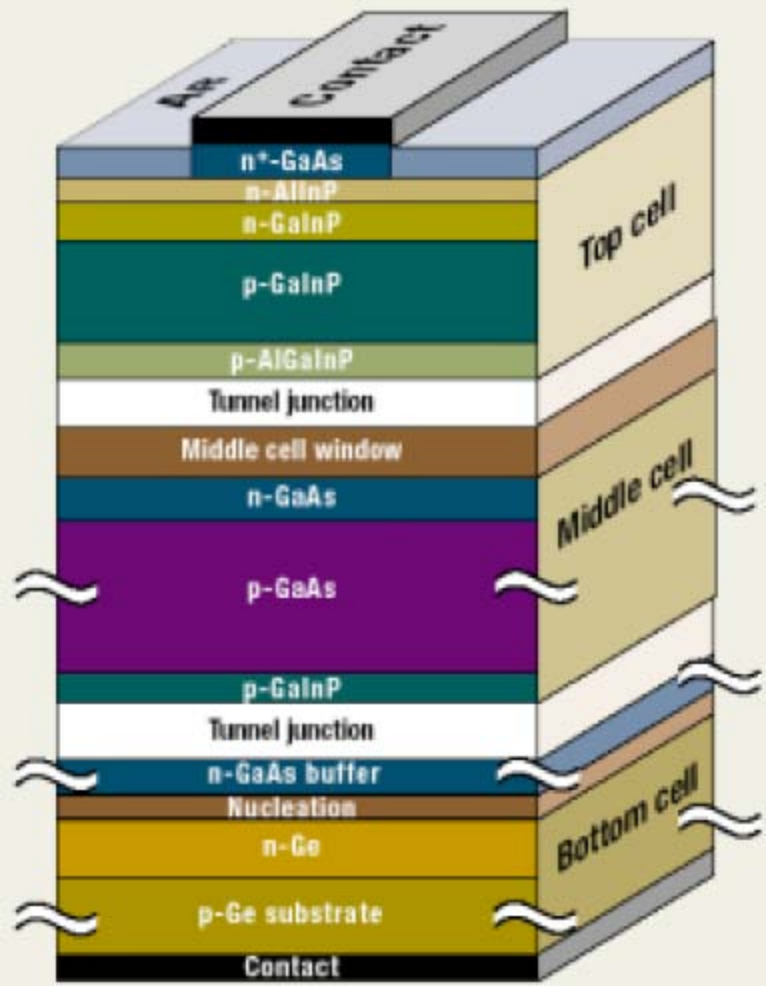
Near-term | Intermediate term | Long term

2000 | 2010 | 2020 | 2030

ORGANIC SOLAR CELLS EFFICIENCIES ABOVE 5%



MULTI-JUNCTION SOLAR CELLS: STATE-OF-THE-ART (WORLDWIDE)



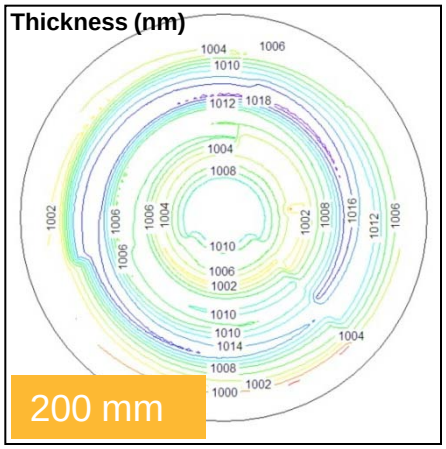
Record conversion efficiencies obtained (32% under 1 sun, 40.1% under concentration)

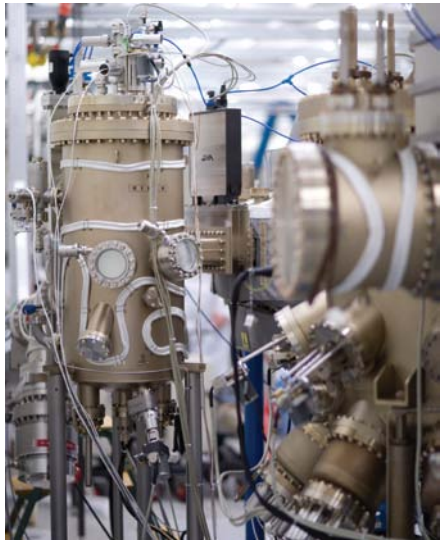
Key technologies:

- current matching of top and middle cell
- wide-gap tunnel junction
- exact lattice matching (1% Indium added in GaAs cell)
- InGaP disordering
- Ge junction formation

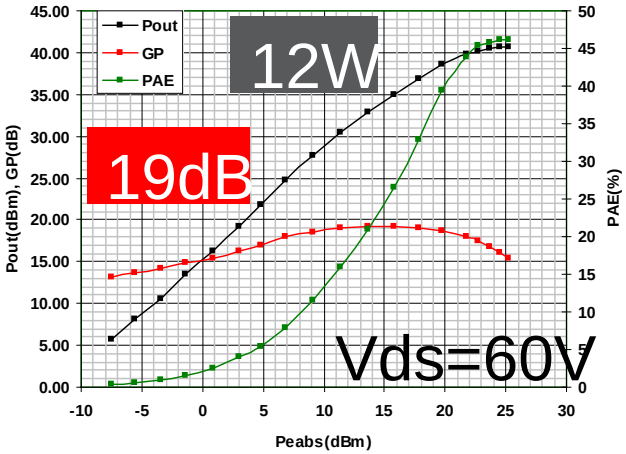
GaN ON Si FOR LOWER COST POWER & LED DEVICES

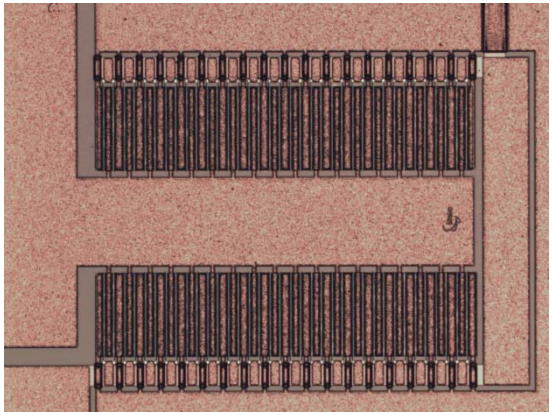
GaN growth on Si



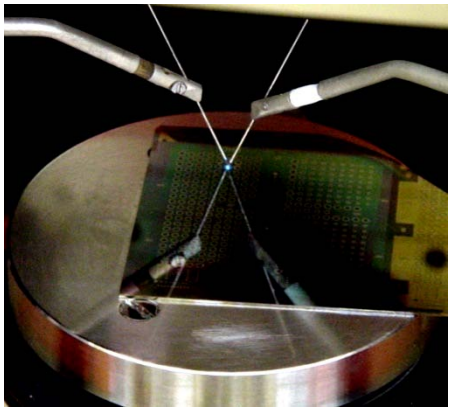


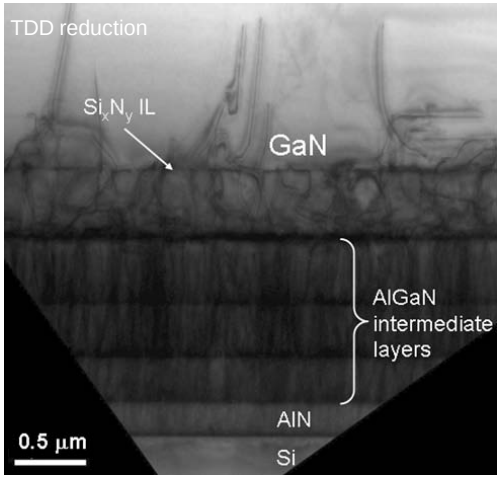
Power HEMTs



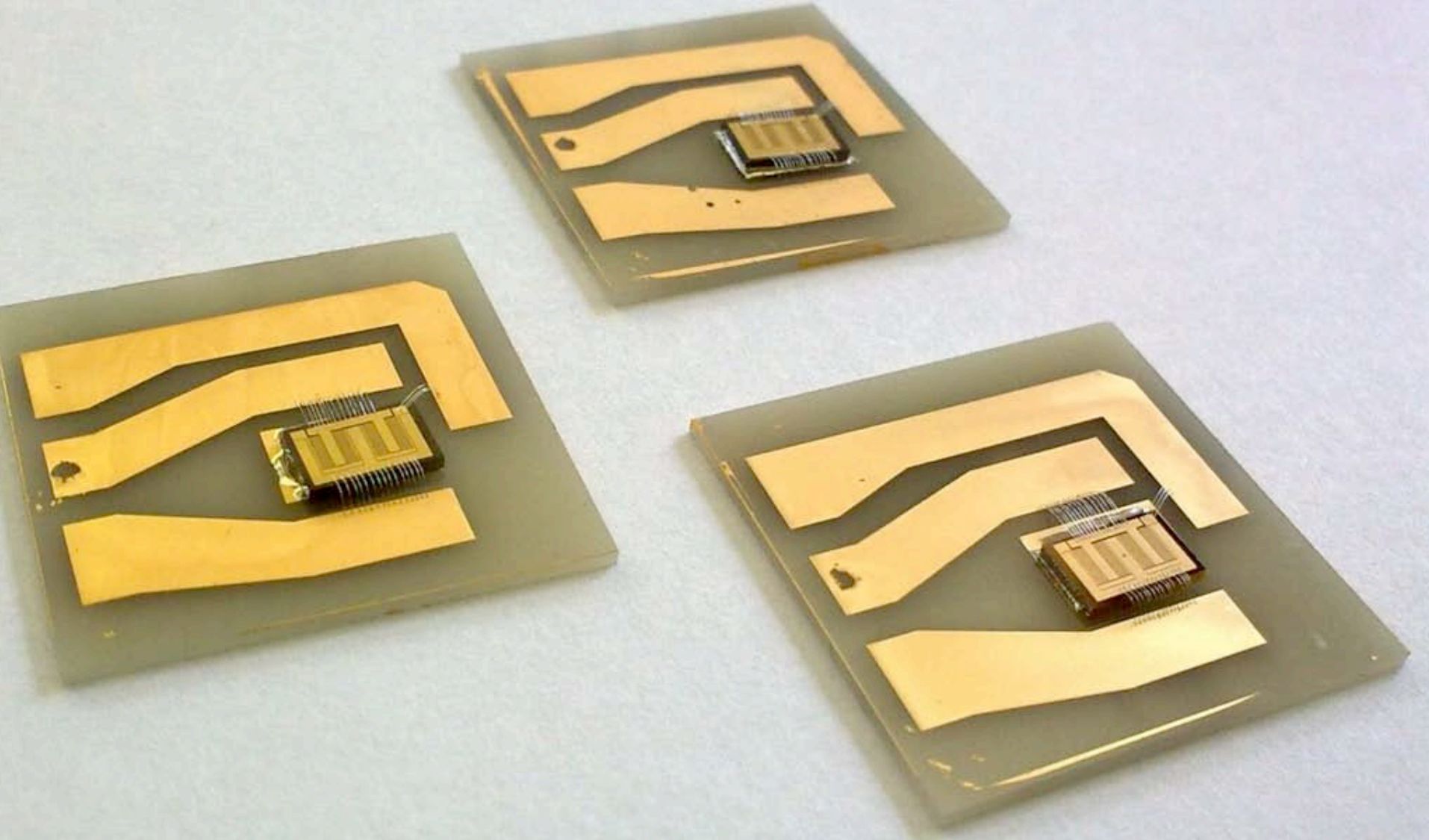


LEDs

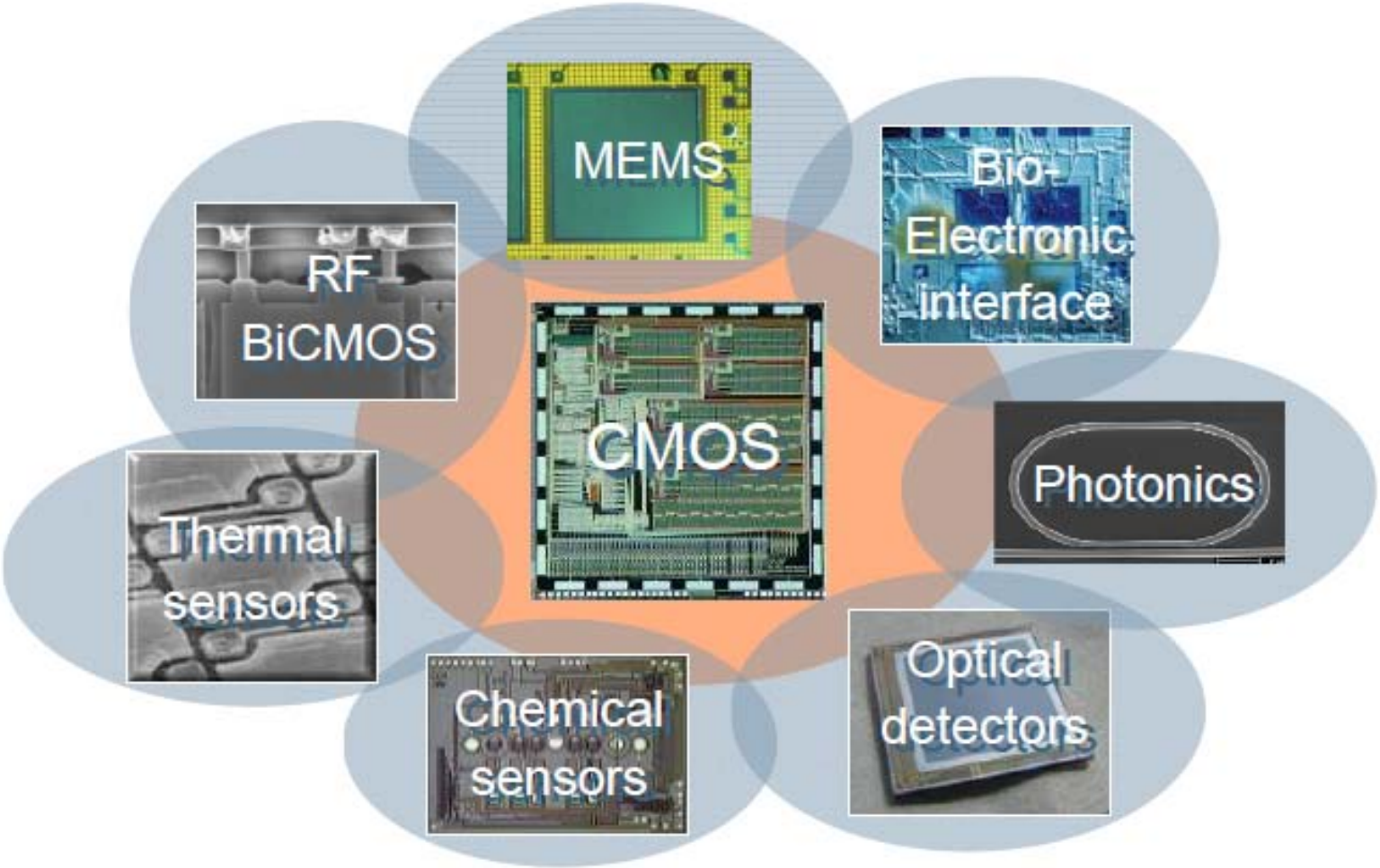




GaN FOR POWER CONVERSION AND SOLID-STATE LIGHTING



CMORE


MEMS
Bio-
Electronic
interface
RF
BiCMOS
CMOS
Photonics
Thermal
sensors
Chemical
sensors
Optical
detectors

ASPIRE
INVENT
ACHIEVE

imec